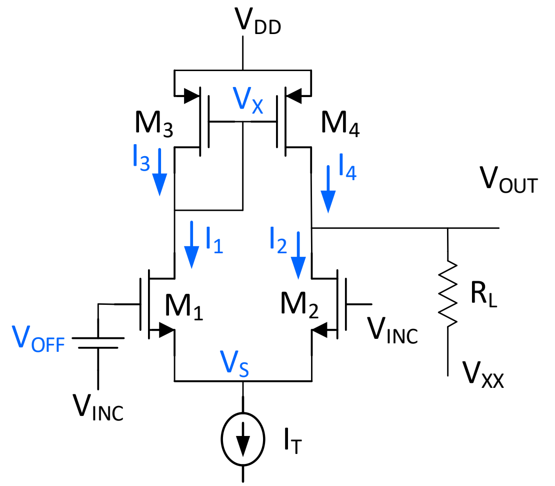
EE 505

Lecture 12

DAC Design

- DAC Architectures
- String DACs

Analysis of Offset Voltage



but

$$\sigma^2_{V_T} = \frac{A^2_{VT0}}{WL} \qquad \sigma^2_{\frac{\mu_R}{\mu_N}} = \frac{A^2_{\mu}}{WL} \qquad \sigma^2_{\frac{C_{OXR}}{C_{OXN}}} = \frac{A^2_{Cox}}{WL} \qquad \sigma^2_{\frac{L_R}{L_N}} = \frac{2A^2_{L}}{WL^2} \qquad \sigma^2_{\frac{W_R}{W_N}} = \frac{2A^2_{W}}{W^2L}$$

So the offset variance can be expressed as

$$\sigma^2_{V_{OFF}} = 2\frac{A^2_{VTn0}}{W_1L_1} + 2\frac{\mu_p L_1}{\mu_n W_1}\frac{A^2_{VTp0}}{L_3^2} + V^2_{EB3}\frac{\mu_p L_1 W_3}{\mu_n L_3 W_1}\frac{1}{2}\left[\frac{A^2_{\mu_n}}{W_3L_3} + \frac{A^2_{\mu_p}}{W_1L_1} + A^2_{Cox}\left(\frac{1}{W_3L_3} + \frac{1}{W_1L_1}\right) + A^2_{W}\left(\frac{2}{W_3^2L_3} + \frac{2}{W_1^2L_1}\right) + A^2_{L}\left(\frac{2}{W_1L_1^2} + \frac{2}{W_3L_3^2}\right)\right]$$

Often this can be approximated by

$$\sigma^2_{V_{OFF}} = 2\frac{A^2_{VTn0}}{W_1L_1} + 2\frac{\mu_p L_1}{\mu_n W_1}\frac{A^2_{VTp0}}{L_3^2} + V^2_{EB3}\frac{\mu_p L_1 W_3}{\mu_n L_3 W_1}\frac{1}{2}\left[\frac{A^2_{\mu_n}}{W_3L_3} + \frac{A^2_{\mu_p}}{W_1L_1} + A^2_{Cox}\left(\frac{1}{W_3L_3} + \frac{1}{W_1L_1}\right)\right]$$

Or even approximated by

$$\sigma^2_{V_{OFF}} = 2\frac{A^2_{VTn0}}{W_1L_1} + 2\frac{\mu_p L_1}{\mu_n W_1}\frac{A^2_{VTp0}}{L_3^2}$$

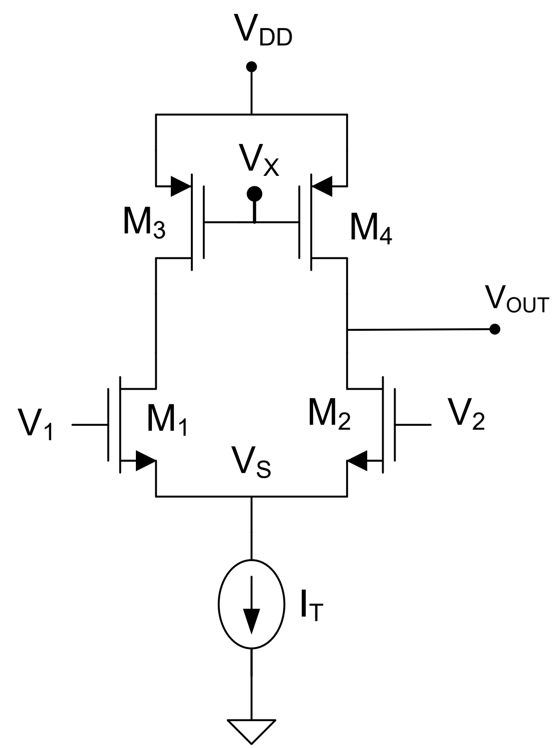
Random Offset Voltages

Correspondingly:

$$\sigma_{V_{OS}}^2 = 2\left[\frac{A_{VTOn}^2}{W_n L_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_n L_p^2}A_{VTOp}^2 + \frac{V_{EBn}^2}{4}\left(\begin{array}{l}\frac{1}{W_n L_n}A_{\mu_n}^2 + \frac{1}{W_p L_p}A_{\mu_p}^2 + A_{COX}^2\left[\frac{1}{W_n L_n} + \frac{1}{W_p L_p}\right] \\ + 2A_L^2\left[\frac{1}{W_n L_n^2} + \frac{1}{W_p L_p^2}\right] + A_w^2\left[\frac{1}{L_n W_n^2} + \frac{1}{L_p W_p^2}\right]\end{array}\right)\right]$$

which again simplifies to

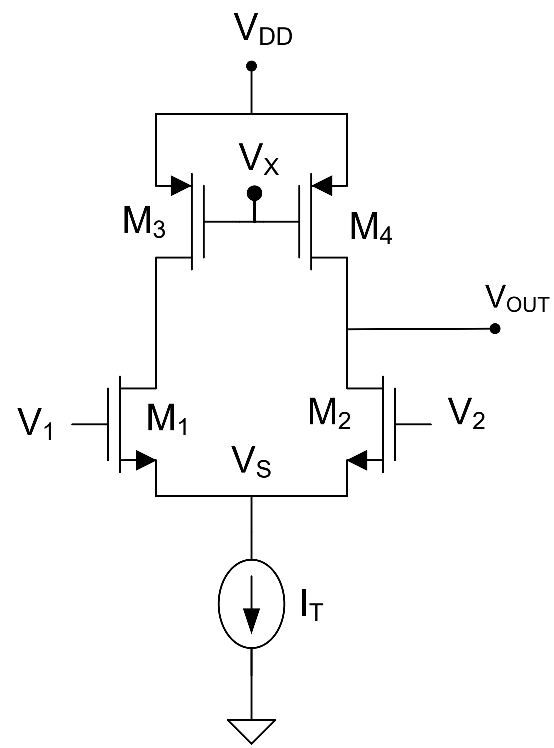
$$\sigma_{V_{OS}}^2 \cong 2\left[\frac{A_{VTO\,n}^2}{W_n L_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_n L_p^2}A_{VTO\,p}^2\right]$$



Note these offset voltage expressions are identical!

Random Offset Voltages

Example: Determine the 3σ value of the input offset voltage for
The MOS differential amplifier is
a) M_1 and M_3 are minimum-sized and
b) the area of M_1 and M_3 are 100 times minimum size



$$\sigma^2_{V_{OS}} \cong 2\left[\frac{A^2_{VTO\,n}}{W_n L_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_n L_p^2}A^2_{VTO\,p}\right]$$

$$\sigma^2_{V_{OS}} \cong \frac{2}{W_n L_n}\left[A^2_{VTO\,n} + \frac{\mu_p}{\mu_n}A^2_{VTO\,p}\right]$$

a)

$$\sigma^2_{V_{OS}} \cong \frac{2}{(0.5\mu)^2}\left[.021^2 + \frac{1}{3}.025^2\right]$$

$$\sigma_{V_{OS}} \cong 72\text{mV}$$

$$3\,\sigma_{V_{OS}} \cong 216\text{mV}$$

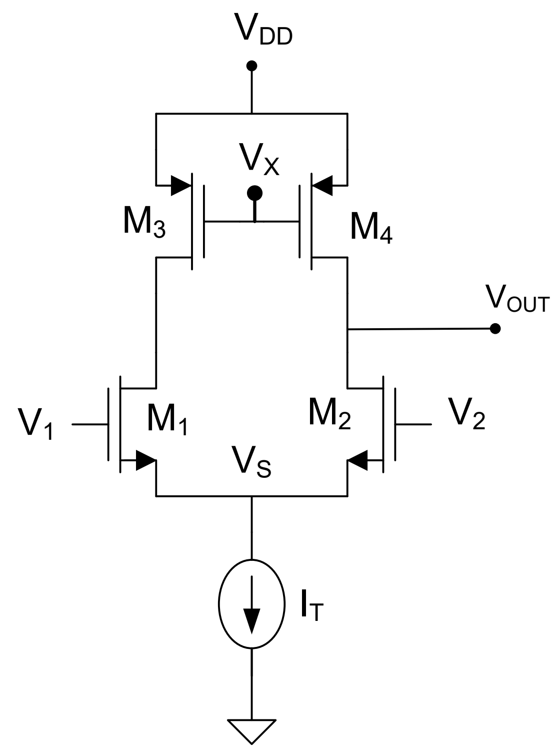
Note this is a very large offset voltage !

Random Offset Voltages

Example: Determine the 3σ value of the input offset voltage for The MOS differential amplifier is

a) M_1 and M_3 are minimum-sized and

b) the area of M_1 and M_3 are 100 times minimum size



$$\sigma^2_{V_{OS}} \cong 2\left[\frac{A^2_{VTO\,n}}{W_n L_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_n L_p^2}A^2_{VTO\,p}\right]$$

$$\sigma^2_{V_{OS}} \cong \frac{2}{W_n L_n}\left[A^2_{VTO\,n} + \frac{\mu_p}{\mu_n}A^2_{VTO\,p}\right]$$

b)

$$\sigma^2_{V_{OS}} \cong \frac{2}{100(0.5\mu)^2}\left[.021^2 + \frac{1}{3}.025^2\right]$$

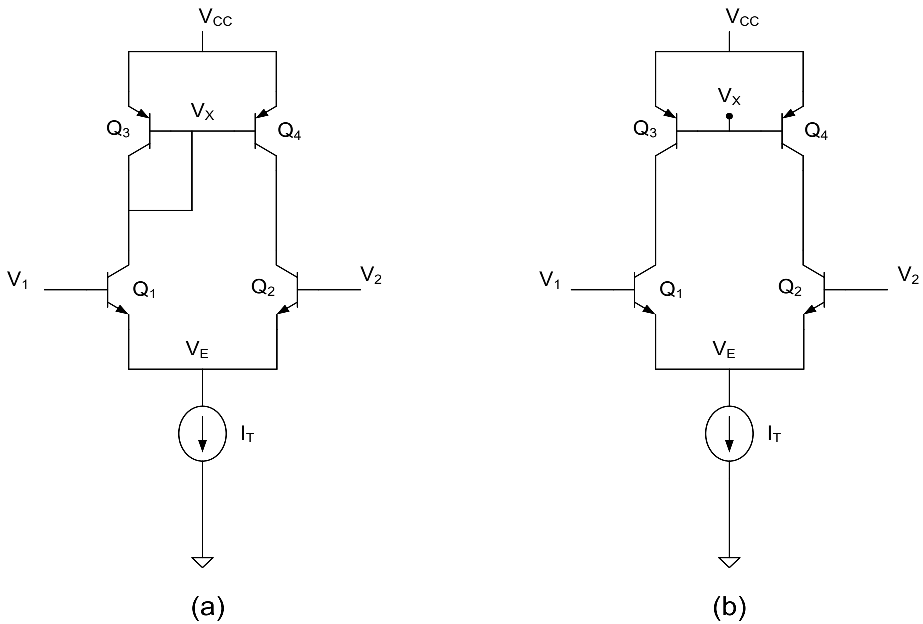
$$\sigma_{V_{OS}} \cong 7.2\text{mV}$$

$$3\,\sigma_{V_{OS}} \cong 21.6\text{mV}$$

Note this is much lower but still a large offset voltage !

The area of M_1 and M_3 needs to be very large to achieve a low offset voltage

Random Offset Voltages



It can be shown that

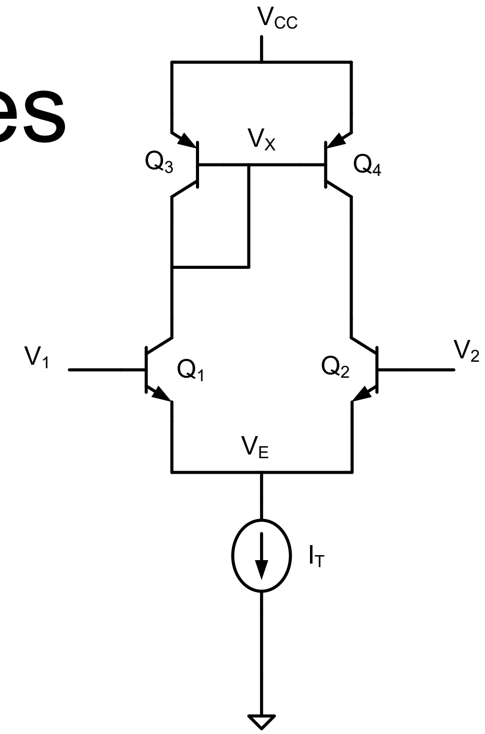
$$\sigma_{V_{OS}}^2 \cong 2V_t^2\left[\frac{A_{Jn}^2}{A_{En}}+\frac{A_{Jp}^2}{A_{Ep}}\right]$$

where very approximately

$$A_{Jn} = A_{Jp} = 0.1\mu$$

Random Offset Voltages

Example: Determine the 3σ value of the offset voltage of a the bipolar input stage if $A_{E1}=A_{E3}=10\mu^2$



$$\sigma_{V_{OS}}^2 \cong 2V_t^2\left[\frac{A_{Jn}^2}{A_{En}}+\frac{A_{Jp}^2}{A_{Ep}}\right]$$

$$\sigma_{V_{OS}} \cong \sqrt{2}V_t\, A_J \frac{\sqrt{2}}{\sqrt{A_E}}$$

$$\sigma_{V_{OS}} \cong 2\bullet 25\text{mV}\bullet 0.1\mu\bullet\frac{1}{\sqrt{10\mu^2}}=1.6\text{mV}$$

$$3\sigma_{V_{OS}} \cong 4.7\text{mV}$$

Note this value is much smaller than that for the MOS input structure !

Random Offset Voltages

Typical offset voltages:

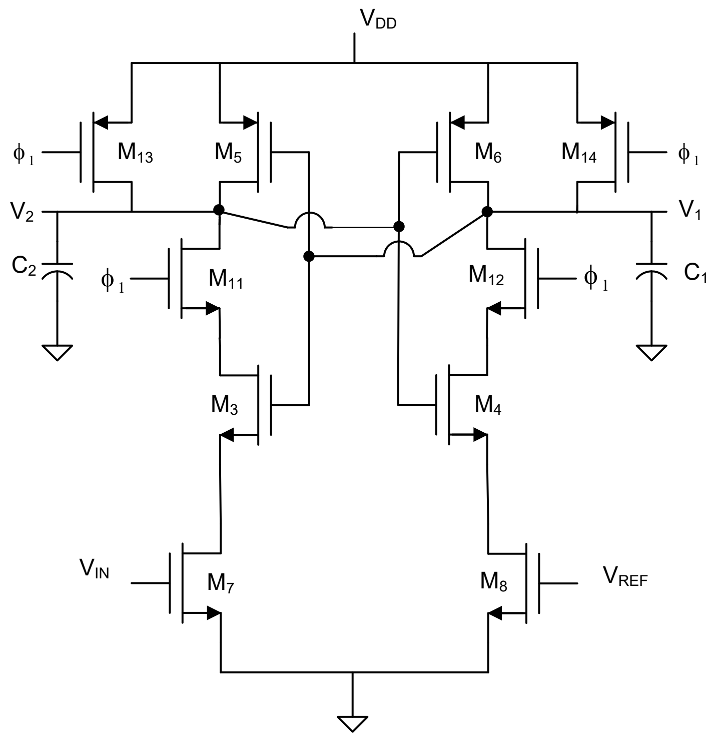
MOS - 5mV to 50MV
BJT - 0.5mV to 5mV

These can be scaled with extreme device dimensions

Often more practical to include offset-compensation circuitry

Dynamic Comparators (Regenerative)

Offset voltage difficult to determine in come classes of comparators



Dynamic clocked comparator

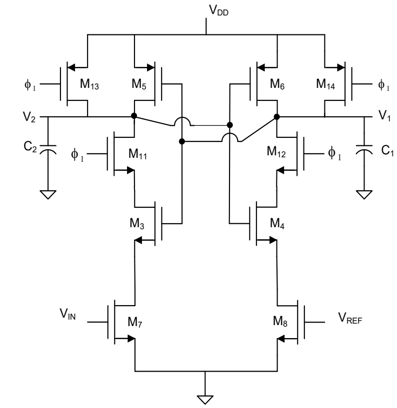
- When φ_1 is low, V_1 and V_2 are precharged to V_{DD} and no static power is dissipated
- When φ_1 is high, enters evaluate state and no static power is dissipated
- Power dissipation almost entirely associated with charging and discharging parasitic capacitors

Review from Last Lecture

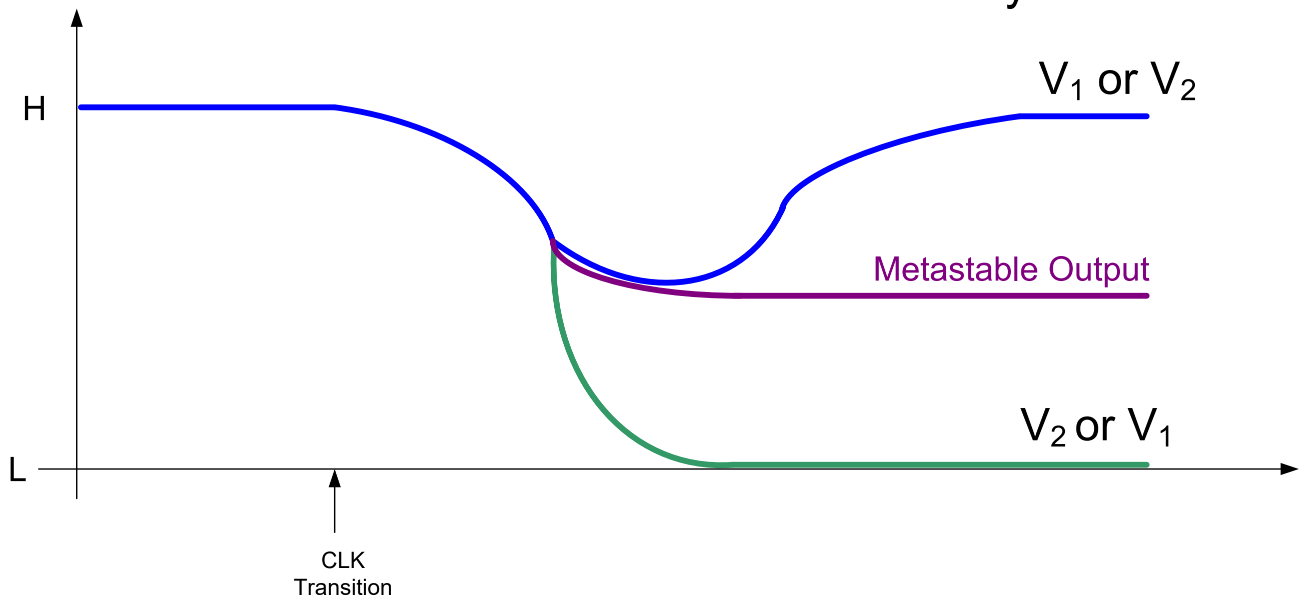
Offset voltage difficult to determine in come classes of comparators

Very small, very fast, low power

But offset voltage can be large (100mV or more)

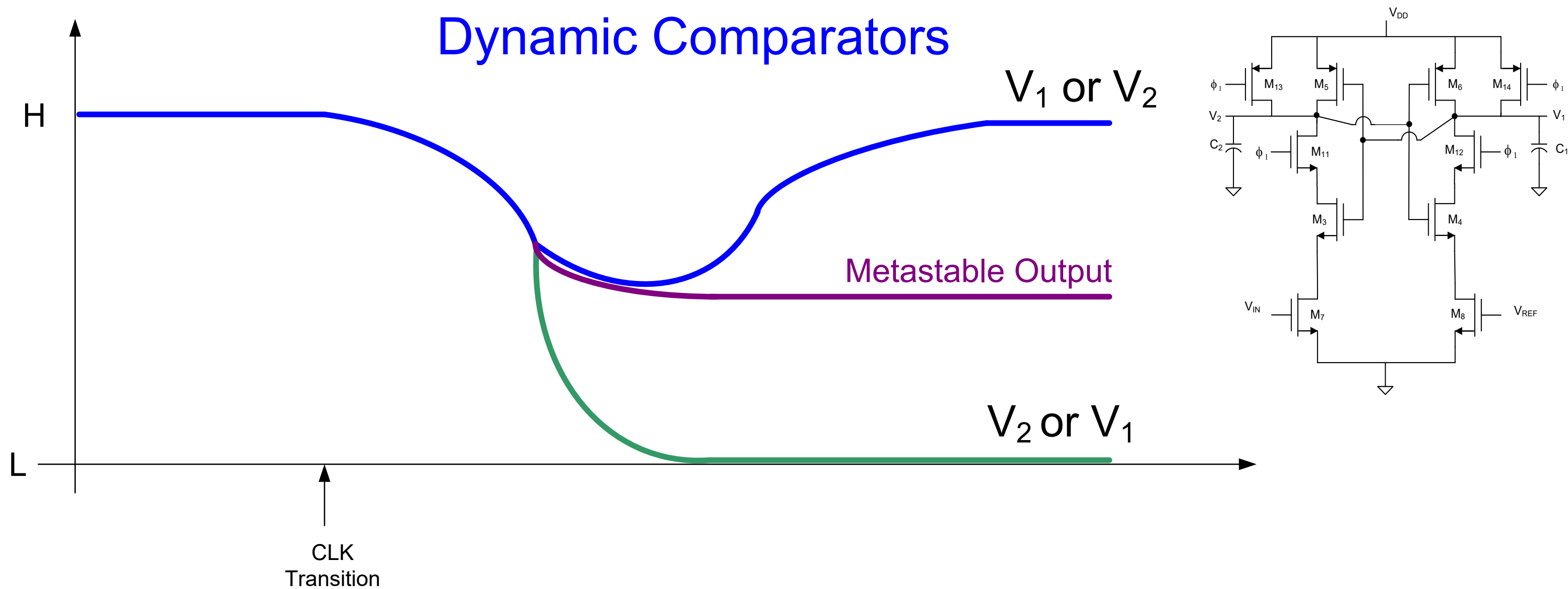


Dynamic clocked comparator



Decision is being made shortly after clock transition when devices are deep in weak inversion and signal levels are very small

Review from Last Lecture



Dynamic Comparators widely used because of low power dissipation

Often include one or more pre-amp stages before regeneration applied

Previous-code dependence and kickback both of concern in dynamic comparators

Noise may significantly affect performance and difficult to analyze and simulate because transient noise models in deep weak inversion are questionable

Still major opportunities to make significant improvement in dynamic comparators

Summary of Offset Voltage Issues

- Random offset voltage is generally dominant and due to mismatch in device and model parameters
- MOS Devices have large V_{OS} if area is small
- σ decreases approximately with $1/\sqrt{A}$
- Multiple fingers for MOS devices offer benefits for common centroid layouts but too many fingers will ultimately degrade offset because perimeter/area ratio will increase (A_W and A_L will become of concern)
- Offset voltage of dynamic comparators is often large and analysis not straightforward
- Offset compensation often used when low offsets important

MOS: $$\sigma^2_{V_{OS}} \cong 2\left[\frac{A^2_{VTO\,n}}{W_n L_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_n L_p^2} A^2_{VTO\,p}\right]$$

Bipolar: $$\sigma^2_{V_{OS}} \cong 2V_t^2\left[\frac{A^2_{Jn}}{A_{En}} + \frac{A^2_{Jp}}{A_{Ep}}\right]$$

DAC Architectures

Types (Nyquist Rate)

- Voltage Scaling
  - Resistor String DACs (string DACs)
  - Interpolating
- Current Steering
  - Binary Weighted Resistors
  - R-2R Ladders
  - Current Source Steering
    - Thermometer Coded
    - Binary Weighted
    - Segmented
- Charge Redistribution
  - Switched Capacitor
- Serial
  - Algorithmic
  - Cyclic or Re-circulating
  - Pipelined
- Integrating
- Resistor Switching
- MDACs (multiplying DACs)

Observations

- Yield Loss is the major penalty for not appropriately managing parasitics and matching and this loss can be ruthless

- The ultimate performance limit of essentially all DACs is the yield loss associated with parasitics and matching

- Many designers do not have or use good statistical models that accurately predict data converter performance

- If you work of a company that does not have good statistical device models
  - Convince model groups of the importance of developing these models
  - (or) develop appropriate test structures to characterize your process

- Existing nonlinear device models may not sufficiently accurately predict device nonlinearities for high-end data converter applications

DAC Architectures

Structures

- Hybrid or Segmented
- Mode of Operation
  - Current Mode
  - Voltage Mode
  - Charge Mode
- Self-Calibrating
  - Analog Calibration
    - Foreground
    - Background
  - Digital Calibration
    - Foreground
    - Background
  - Dynamic Element Matching
- Laser or Link Trimmed
- Thermometer Coded or Binary
- Radix 2 or non-radix 2
- Inherently Monotone

DAC Architectures

- Type of Classification may not be unique nor mutually exclusive
- Structure is not mutually exclusive
- All approaches listed are used (and probably some others as well)
- Some are much more popular than others
  - Popular Architectures
    - Resistor String (interpolating)
    - Current Source Steering (with segmentation)
    - Charge Redistribution
- Many new architectures are possible and some may be much better than the best currently available
- All have perfect performance if parasitic and matching performance are ignored !
- Major challenge is in determining appropriate architecture and managing the parasitics

Nonideal Effects of Concern

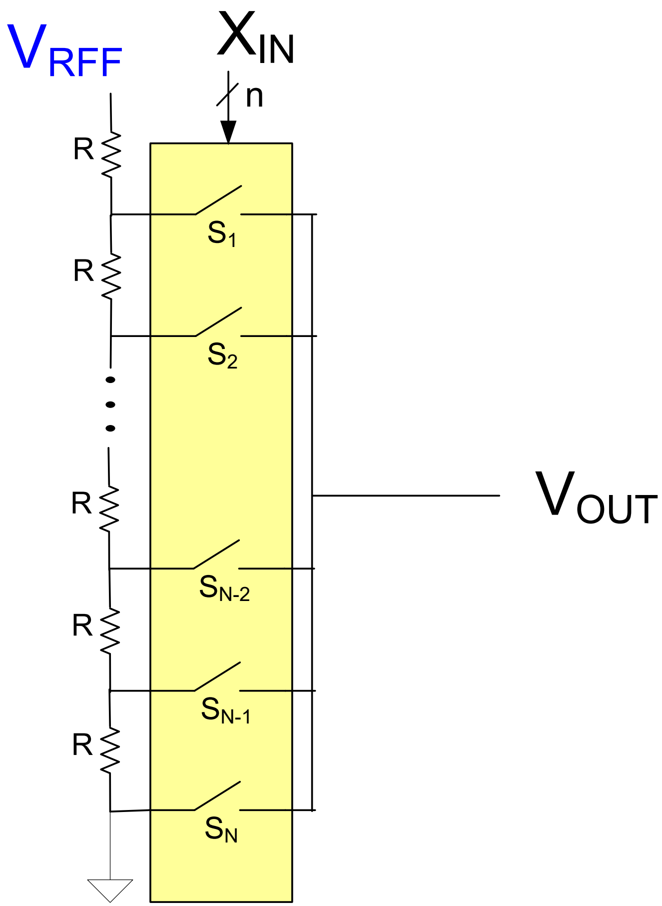
- Matching
- Parasitic Capacitances
  (including Charge injection)
- Loading
- Nonlinearities
- Interconnect resistors
- Noise
- Speed
- Jitter
- Temperature Effects
- Aging
- Package stress

Observations

- Experienced Designers/Companies often produce superior data converter products
- Essentially all companies have access to the same literature, regularly reverse engineer successful competitors products and key benefits in successful competitors products are generally not locked up in patents
- High-end designs(speed and resolution) may get attention in the peer community but practical moderate performance converters usually make the cash flow
- Area (from a silicon cost viewpoint) is usually not the driving factor in high-end designs where attractive price/mfg cost ratios are common
- Considerable ongoing demand for data converter designers – particularly in ASICs where DAC optimized for specific application

DAC Architectures

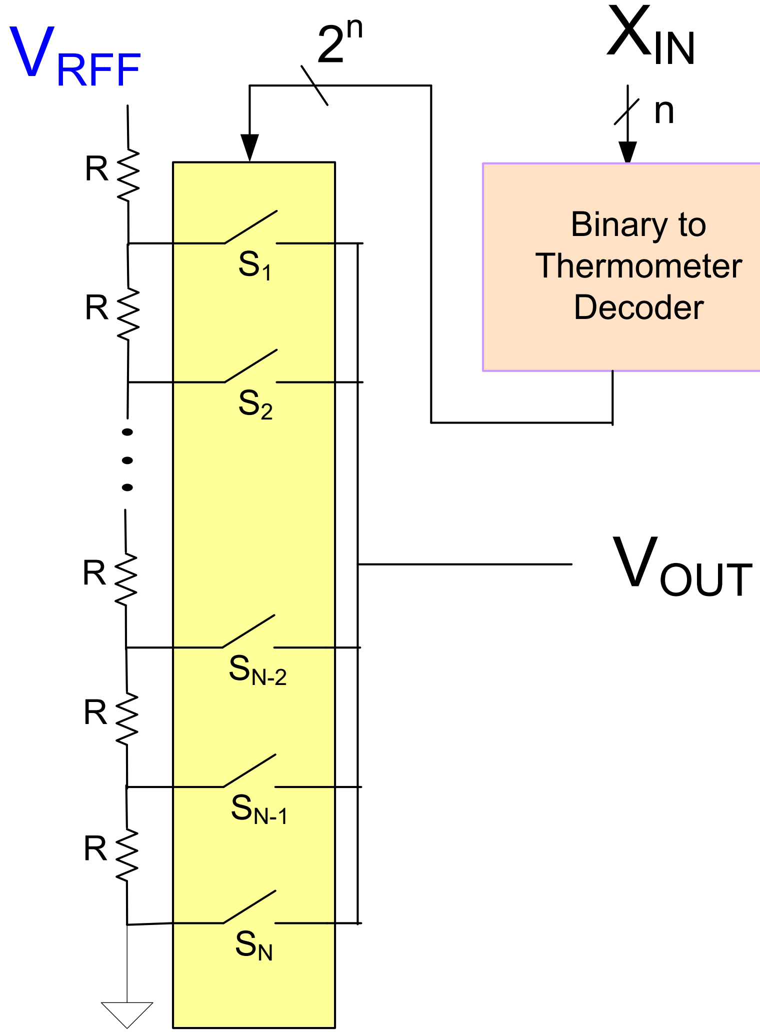
R-String



X_{IN} is decoded to close one switch

DAC Architectures

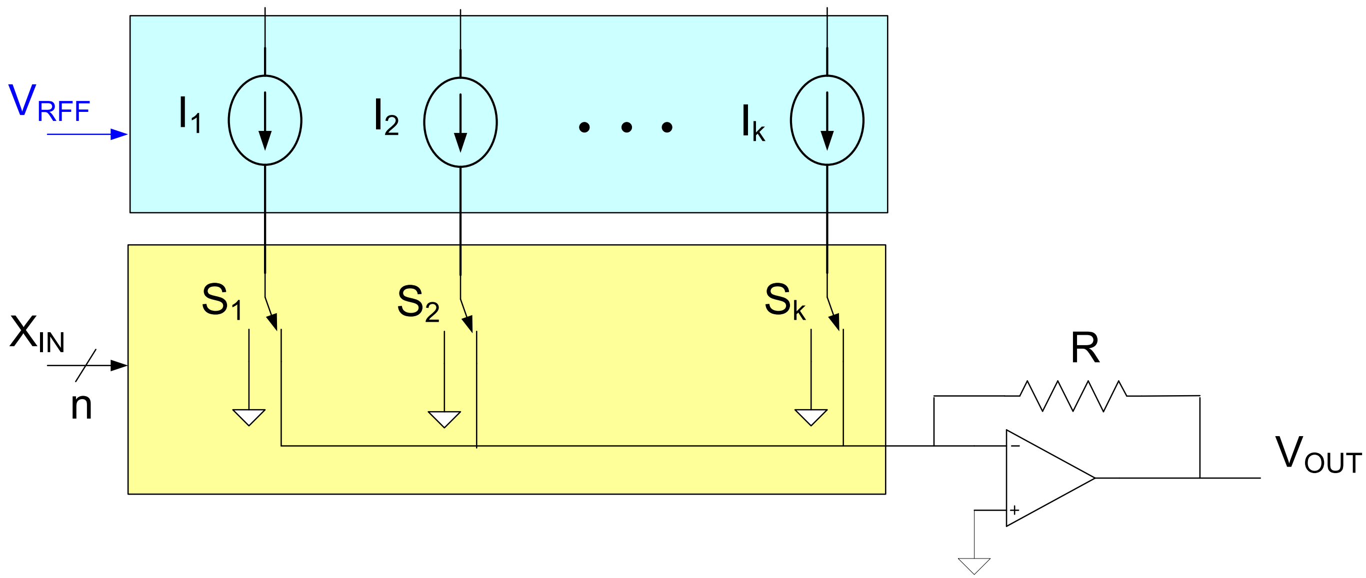
R-String



Basic R-String DAC including Logic to Control Switches

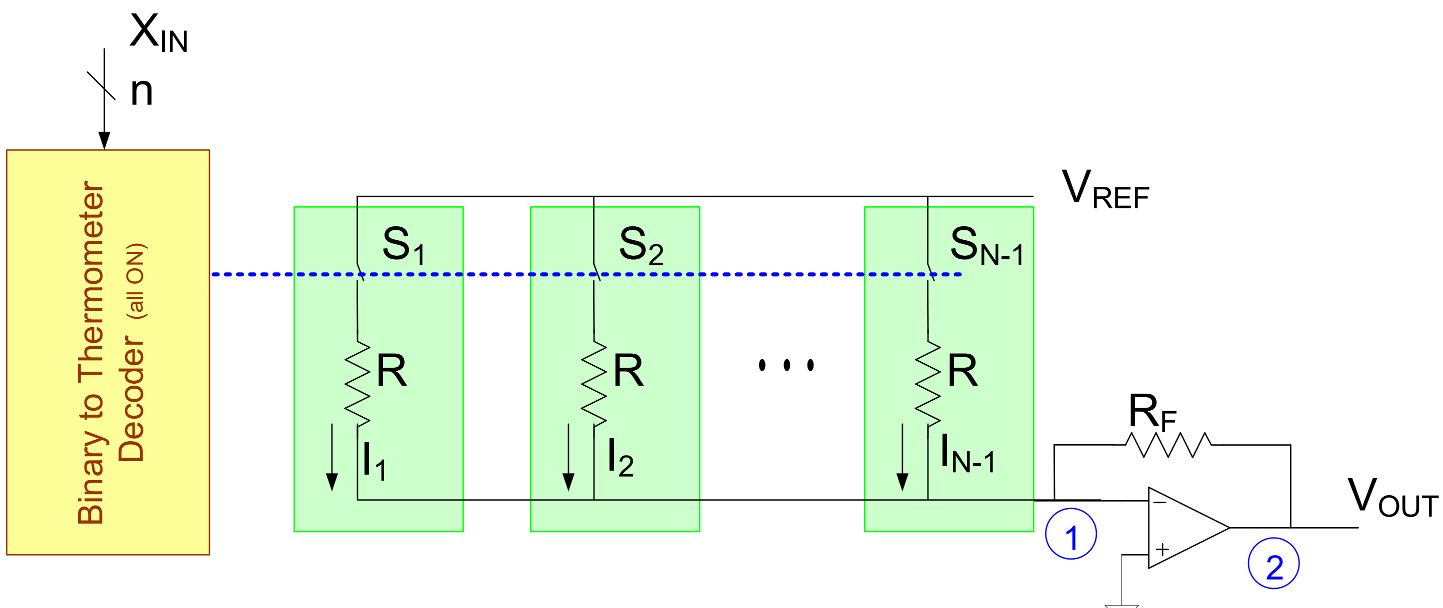
DAC Architectures

Current Steering



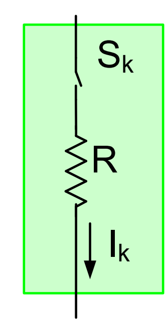
DAC Architectures

Current Steering



Inherently Insensitive to Nonlinearities in Switches and Resistors

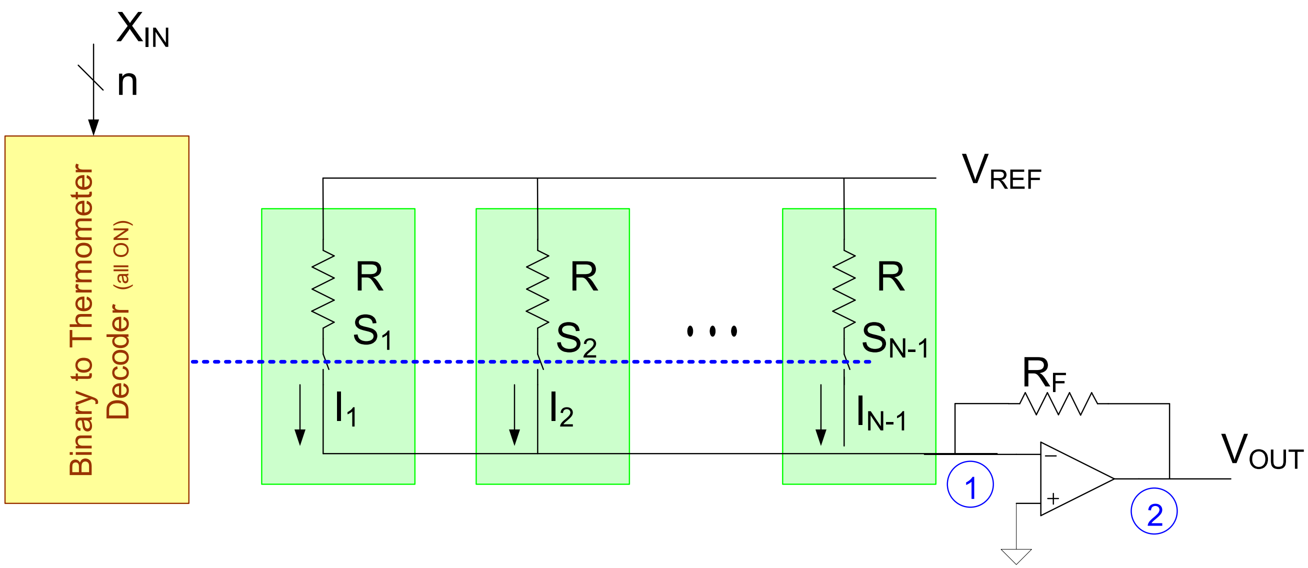
- Termed "top plate switching"
- Thermometer coded
- Based upon unary cell
- Speed limited by Op Amp and clock transients
- Device count becomes impractical for large N



Unary bit cell

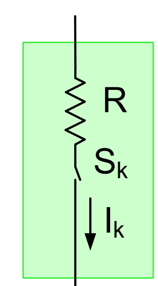
DAC Architectures

Current Steering



Inherently Insensitive to Nonlinearities in Switches and Resistors
Smaller ON resistance and less phase-shift from clock edges

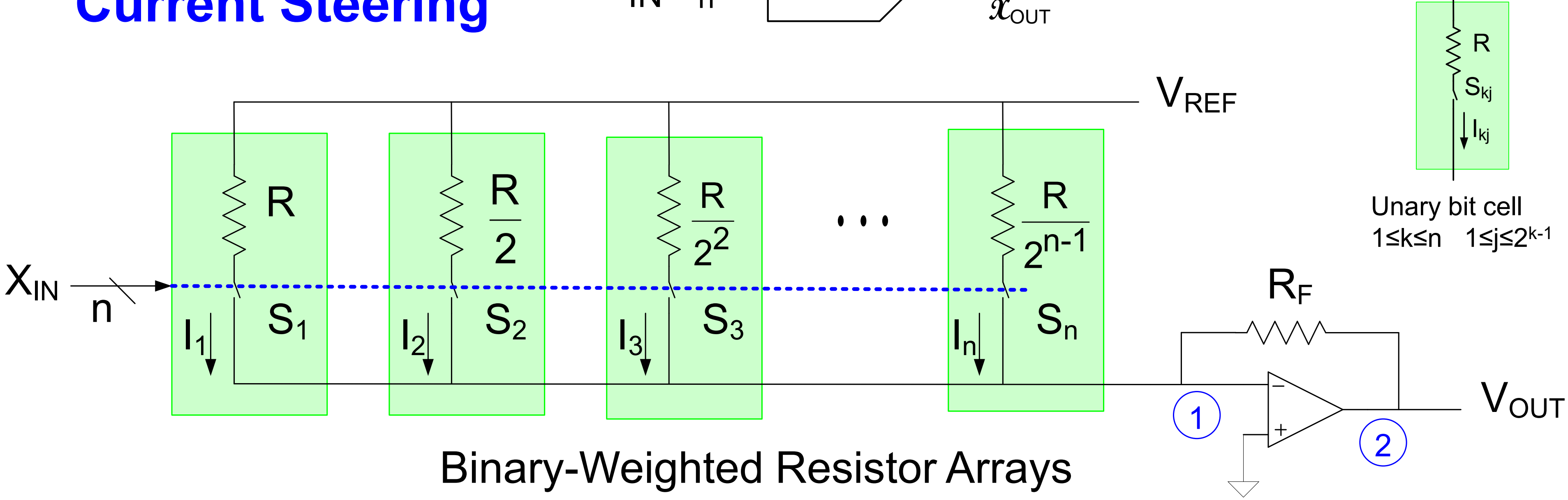
- Termed “bottom plate switching”
- Thermometer coded
- Based upon unary cell
- Speed limited by Op Amp
- Device count becomes impractical for large N



Unary bit cell

DAC Architectures

Current Steering



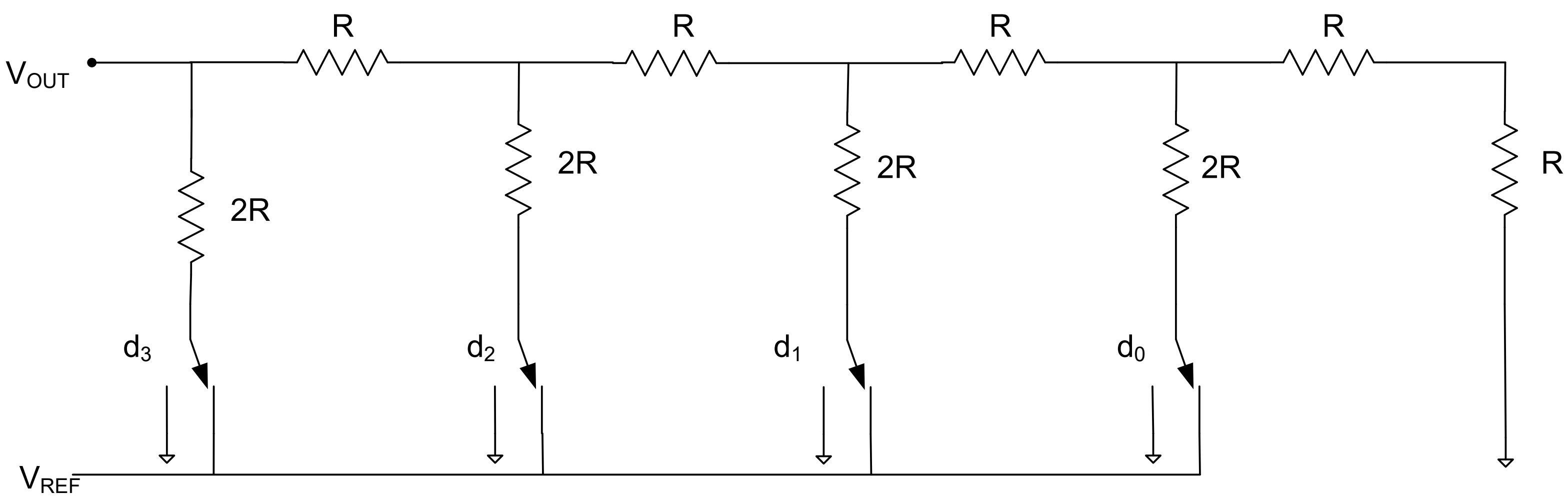
Binary-Weighted Resistor Arrays

- Unary bit cells usually bundled to make resistors
- Same number of unary cells needed as for thermometer coded structure
- Need for decoder eliminated !
- DNL may be a major problem
- INL performance about same as thermometer coded if same unit resistors used
- Sizing and layout of switches is critical

Observe thermometer coding and binary weighted both offer some major advantages and some major limitations

DAC Architectures

R-2R (one variant) (4-bits shown)



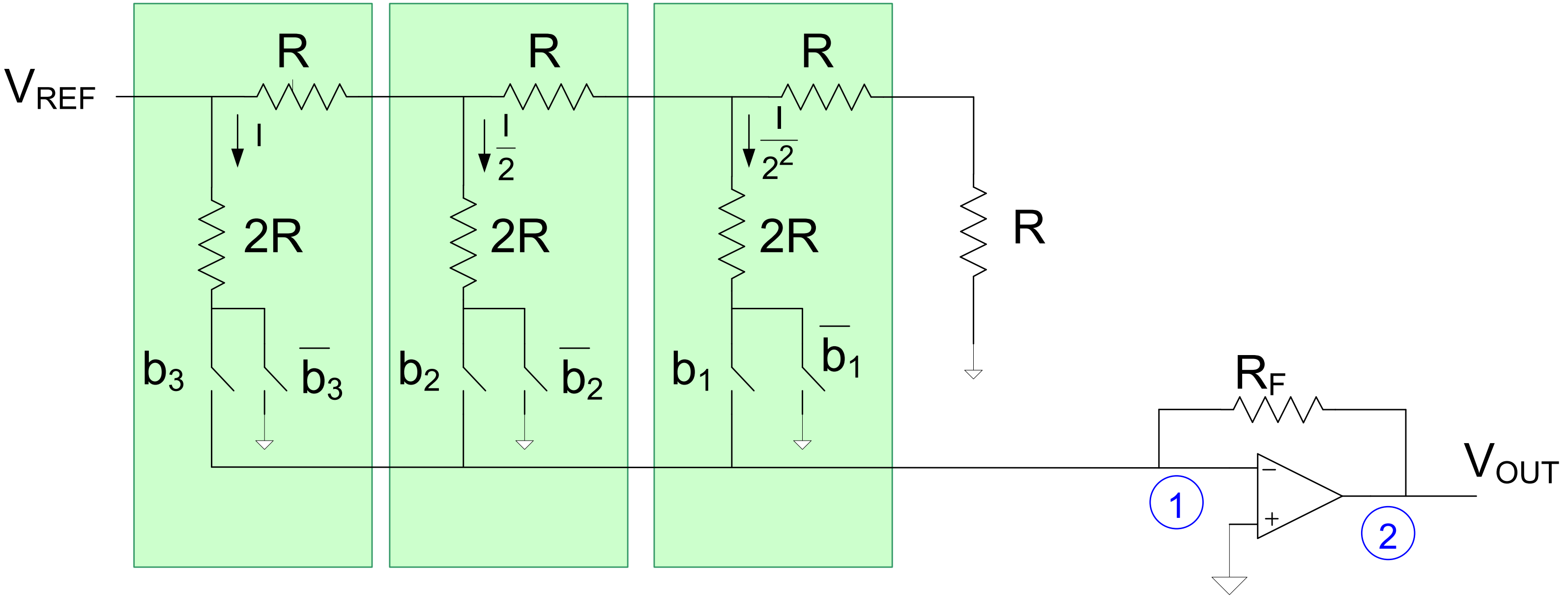
By superposition:

$$V_{OUT} = V_{REF} d_3 \bullet \frac{1}{2} + V_{REF} d_2 \bullet \frac{1}{4} + V_{REF} d_1 \bullet \frac{1}{8} + V_{REF} d_0 \bullet \frac{1}{16} = V_{REF} \sum_{k=0}^{3} \frac{d_k}{2^{4-k}} = V_{REF} \sum_{k=1}^{4} \frac{d_{4-k}}{2^k}$$

DAC Architectures

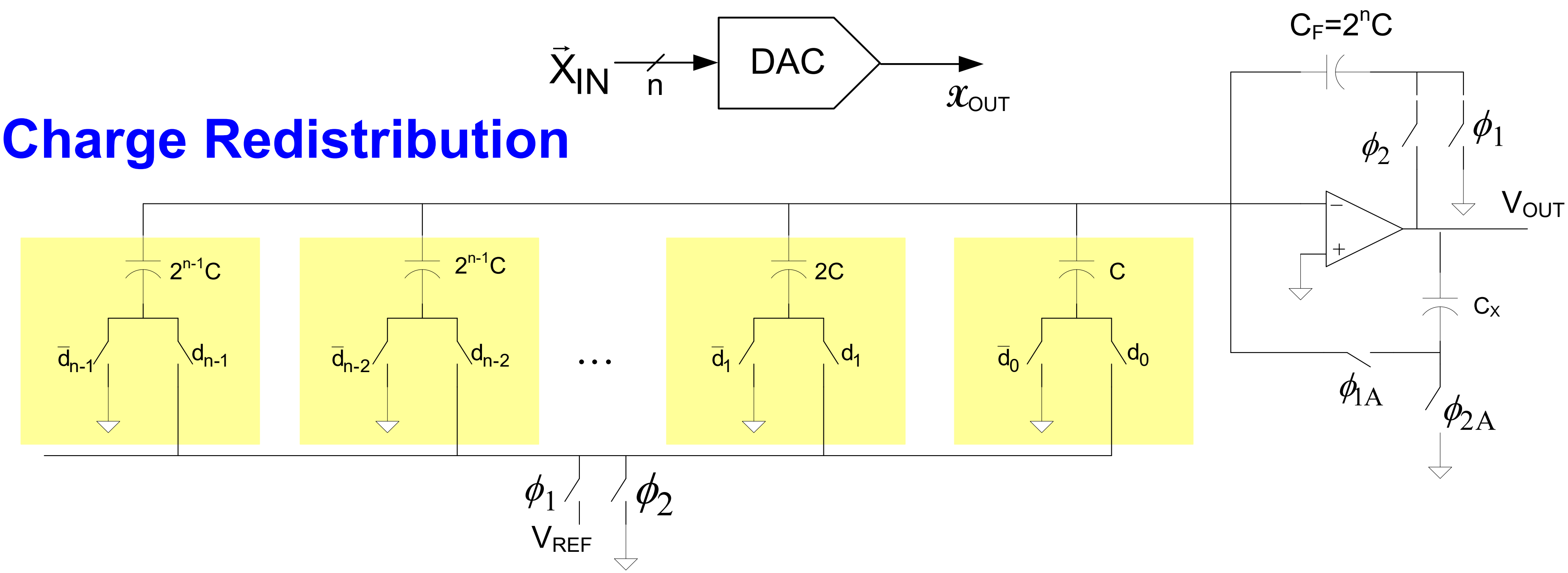
Current Steering

R-2R (another variant)

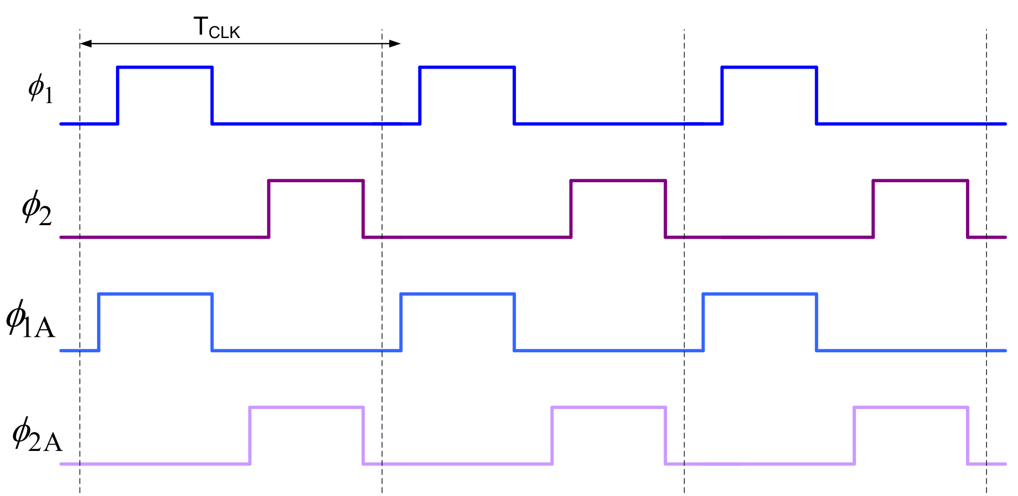


R-2R Resistor Arrays

DAC Architectures



Charge Redistribution



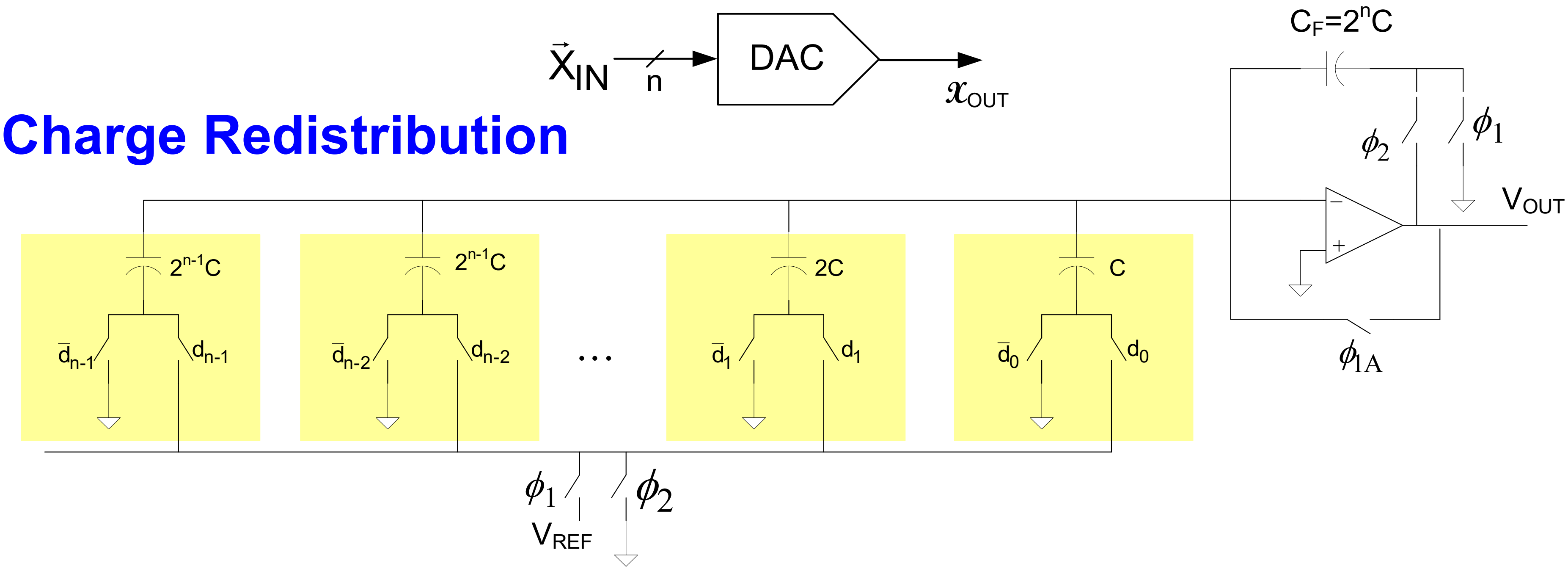
Unary cell used for capacitor array

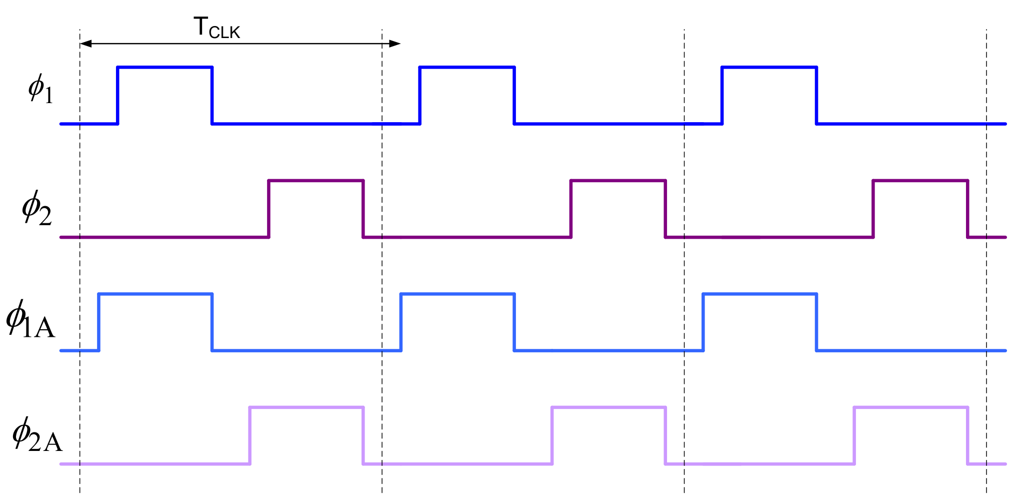
C_X does some good things
(mitigates V_{OS}, 1/f noise and finite gain errors)

Will not consider C_X affects at this time

DAC Architectures

Charge Redistribution



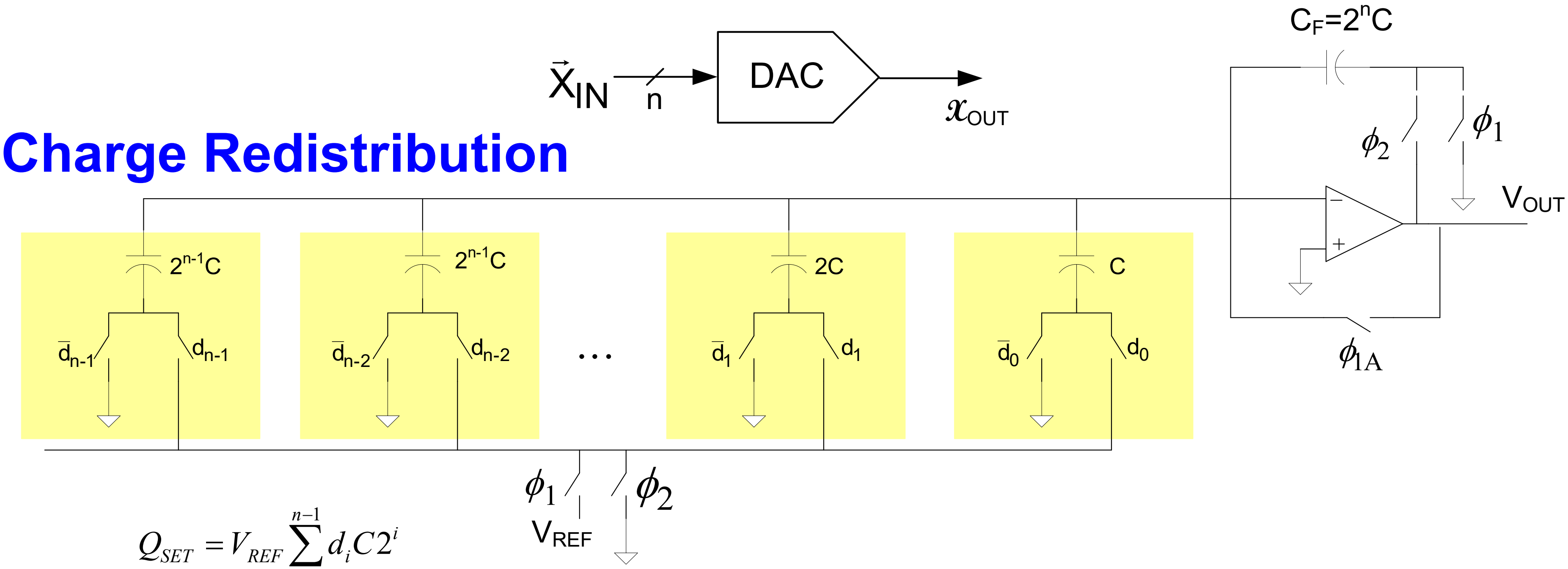


Unary cell used for capacitor array

Common-mode input of OA is fixed

DAC Architectures

Charge Redistribution



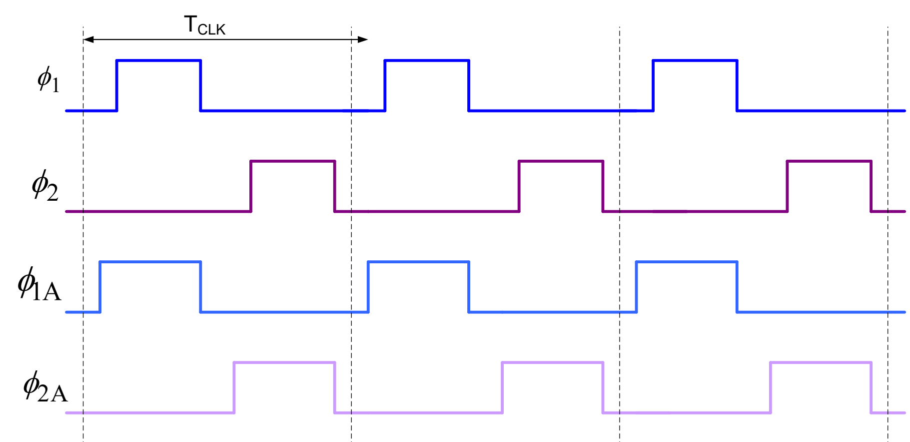
$$Q_{SET} = V_{REF}\sum_{i=0}^{n-1} d_i C 2^i$$

$$Q_{RDIS} = V_{OUT}\, 2^n C$$

$$Q_{SET} = Q_{RDIS}$$

$$V_{REF}\sum_{i=0}^{n-1} d_i C 2^i = V_{OUT}\, 2^n C$$

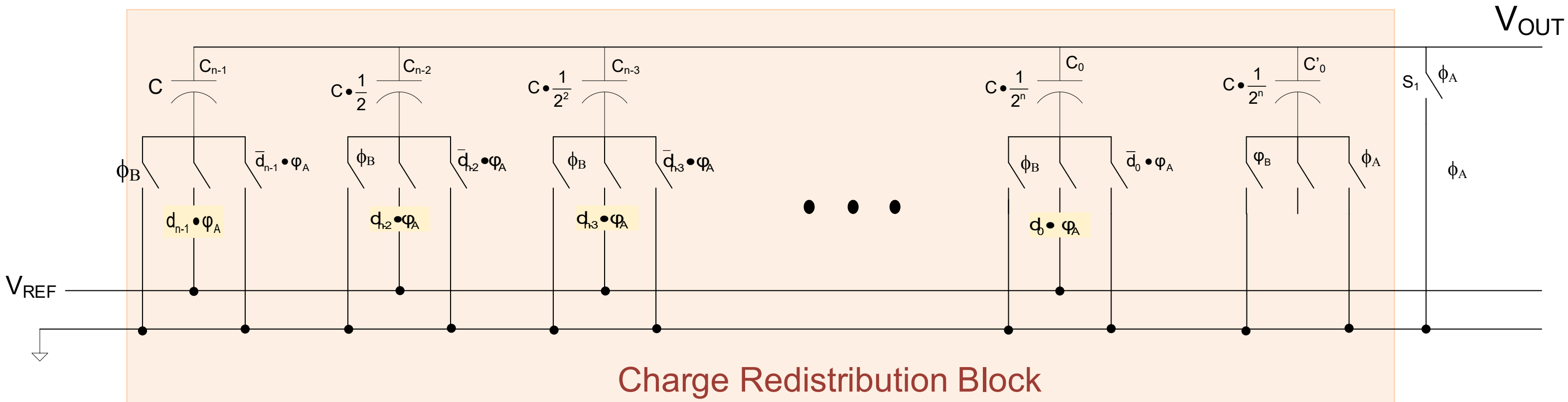
$$V_{OUT} = V_{REF}\sum_{i=0}^{n-1} d_i 2^{i-n}$$



Note capacitor values play no role in this analysis, only capacitor ratios

DAC Architectures

Charge Redistribution



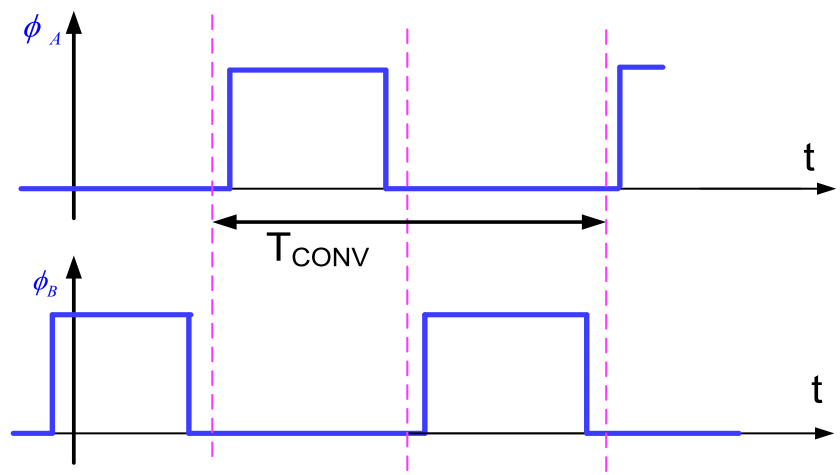
$$Q_{SET} = V_{REF} \sum_{i=0}^{n-1} d_i \frac{C}{2^{n-i}}$$

$$Q_{RDIS} = V_{OUT}\left(\sum_{i=0}^{n-1} C_i + \left[C_0^{'}\right]\right) = V_{OUT}\left(\sum_{i=0}^{n-1} \frac{C}{2^{n-i}} + \left[\frac{C}{2^n}\right]\right) = V_{OUT} C$$

$$Q_{SET} = Q_{RDIS}$$

$$V_{REF} \sum_{i=0}^{n-1} d_i \frac{C}{2^{n-i}} = V_{OUT} C$$

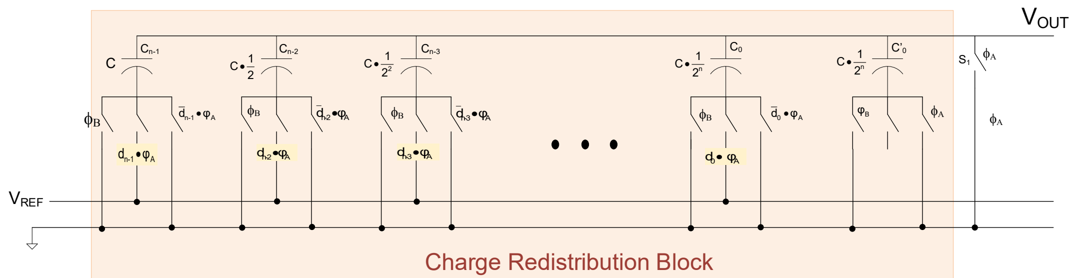
$$V_{OUT} = V_{REF} \sum_{i=0}^{n-1} d_i 2^{i-n}$$



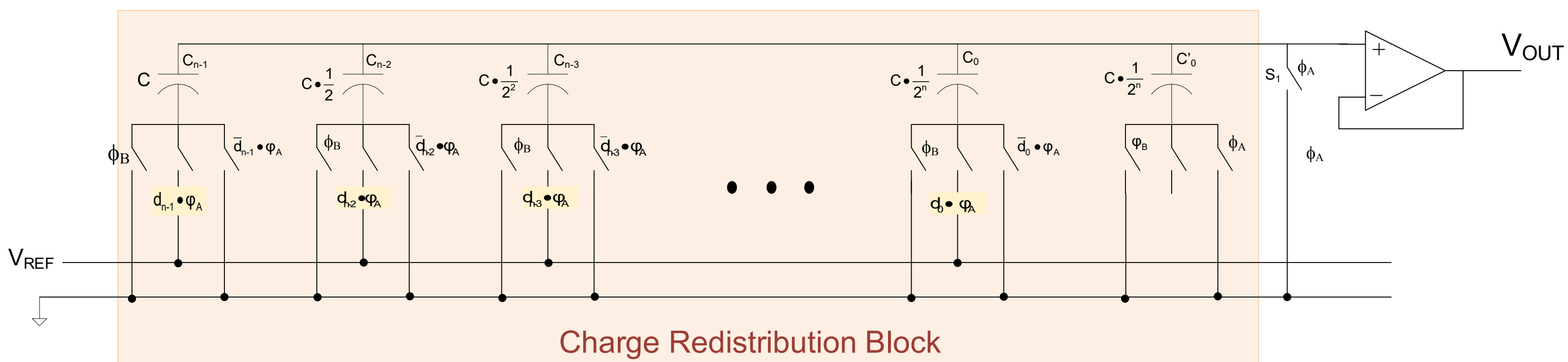
Note capacitor values play no role in this analysis, only capacitor ratios

DAC Architectures

Charge Redistribution



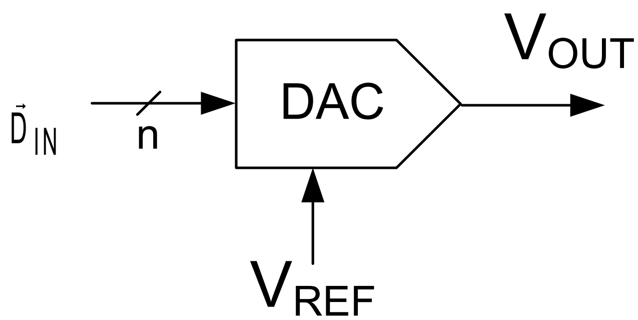
Not limited by speed of Op Amp (no feedback!)
Loading of output will affect charge redistribution
Often use buffer at output

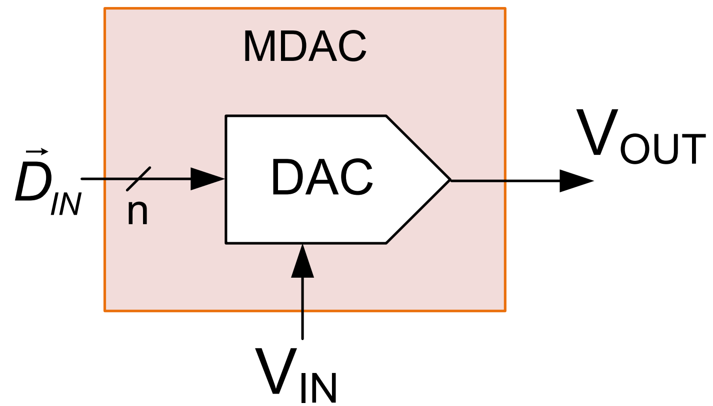


Limited by speed of Op Amp
Op Amp Common-Mode Input Range can be large

DAC Architectures

MDAC (Multiplying DAC)





V_{REF} fixed or limited range

$$V_{OUT} = V_{REF} \bullet \left[\vec{D}_{IN}\right]_{DECIMAL}$$

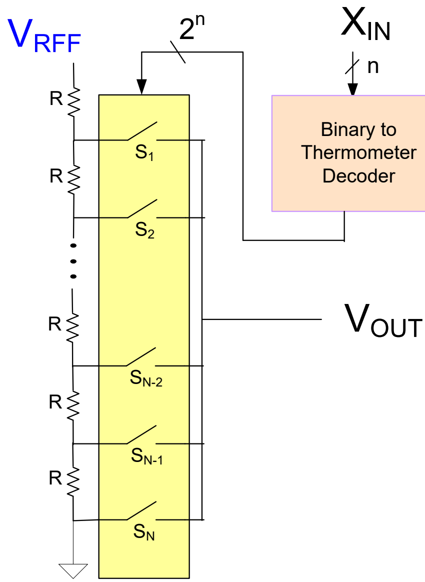
V_{IN} Variable, often positive or negative

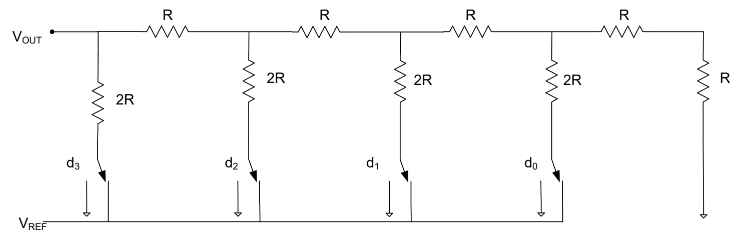
$$V_{OUT} = V_{IN} \bullet \left[\vec{D}_{IN}\right]_{DECIMAL}$$

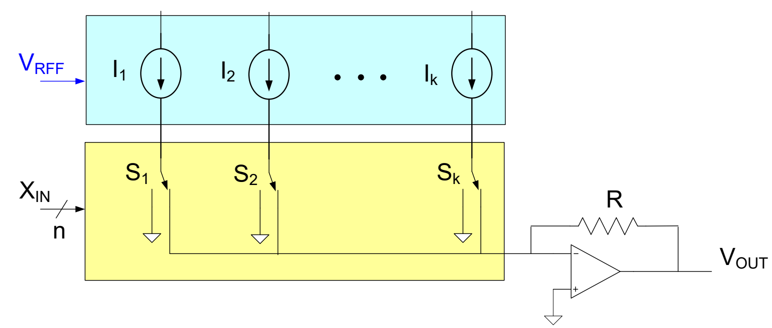
- Some define MDACs to be DAC structures that have current outputs
- Many DAC structures can perform well as a MDAC (possibly one quadrant)
- Performance of some DAC structures limited if V_{REF} is varied

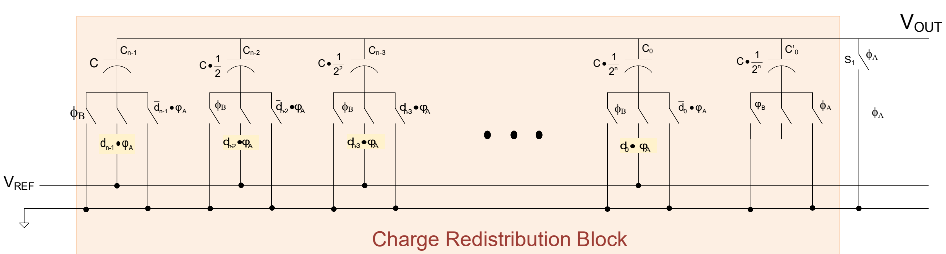
DAC Architectures

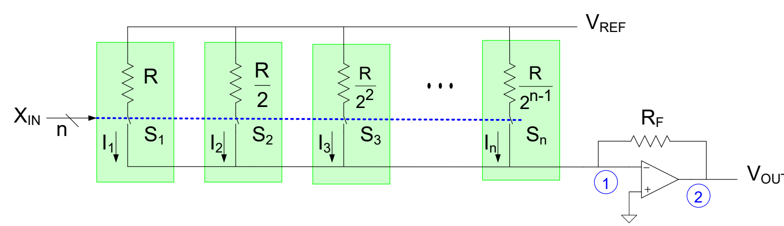
Suitable as MDAC?





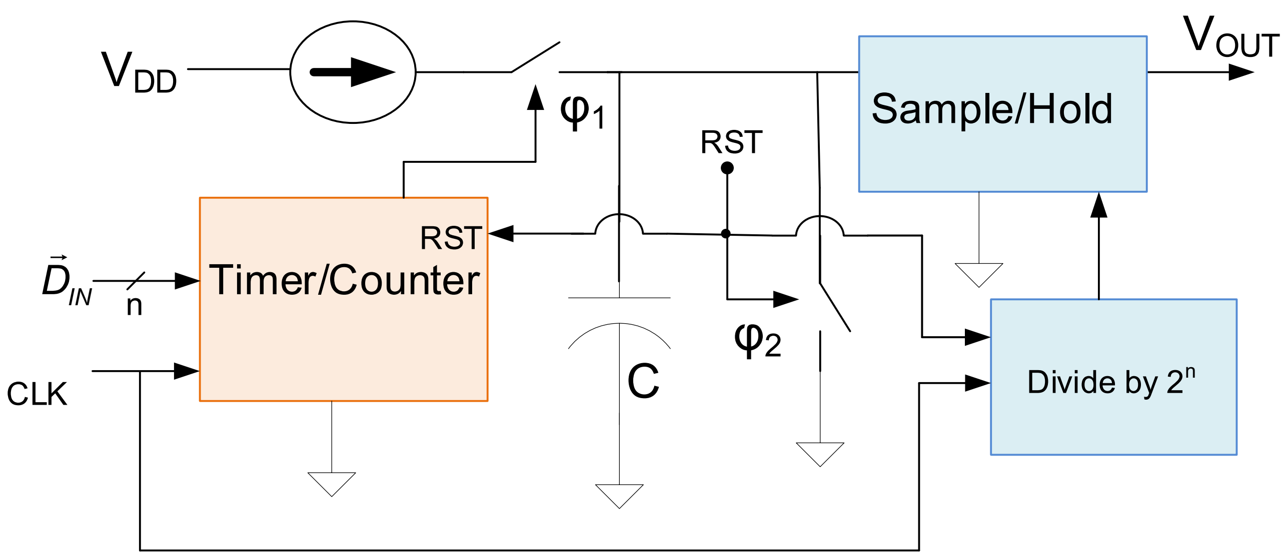






DAC Architectures

Single Slope

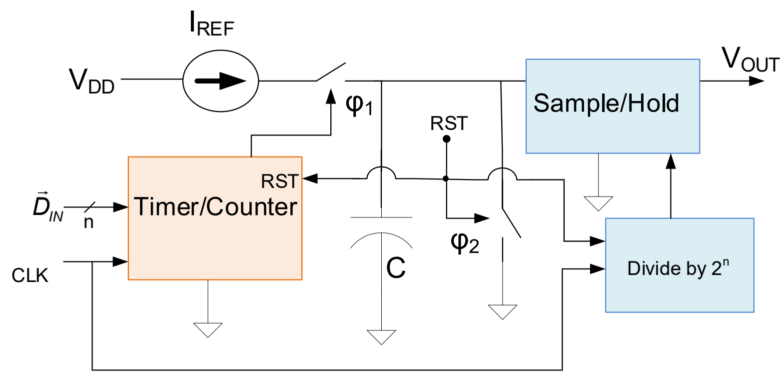


Single-Slope DAC

Is this an MDAC? Yes – but multiplying factor is I_{REF}

DAC Architectures

Single Slope



Single-Slope DAC

Can be viewed as a time-domain DAC where resolution headroom is very large

Benefits of Single-Slope ADC?

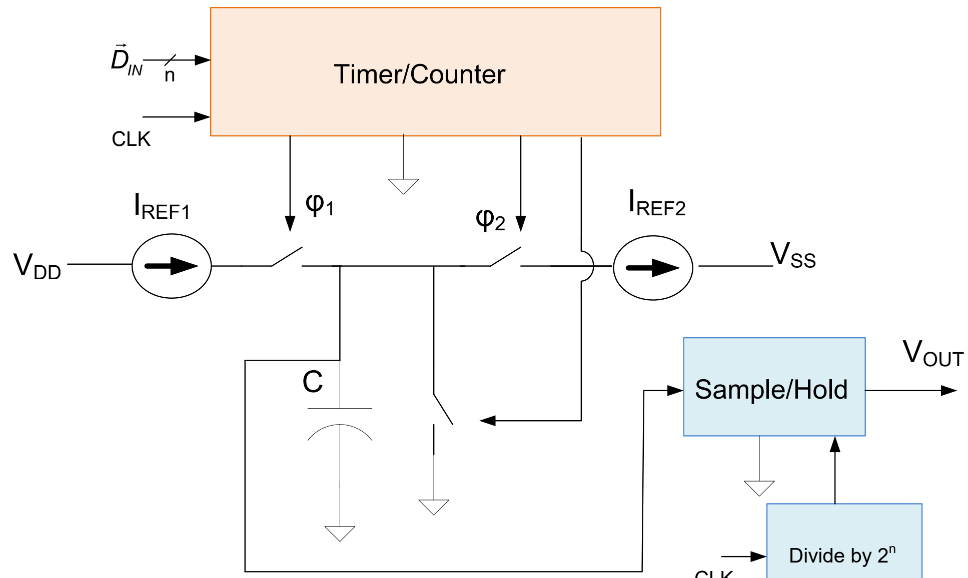
- No matching required
- Very simple structure
- Mostly Digital
- Very low DNL
- Very fine resolution possible
- No previous code dependence
- No binary to thermometer decoder

Limitations of Single-Slope ADC?

- Slow conversion rate
- Large C
- Leakage currents that will be temperature dependent
- Nonlinearity in C?
- Nonlinearity in I_{REF}

DAC Architectures

Dual Slope



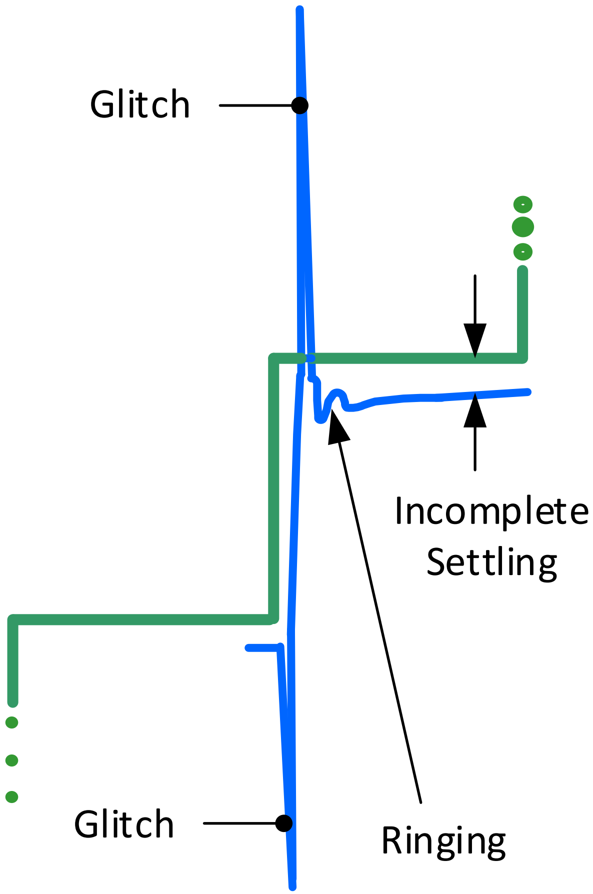
Dual-Slope DAC

Provides DAC with positive and negative outputs

Term “dual slope” means something different here than what we see in “dual slope” ADCs

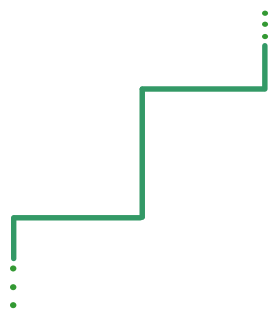
Is this an MDAC? Yes if $I_{REF1}=I_{REF2}=I_{REF}$ but multiplying factor is I_{REF}

DAC Performance Issues and Concerns

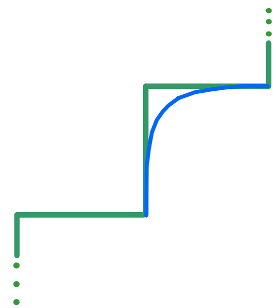


Important to identify how various nonidealities in DAC affect performance

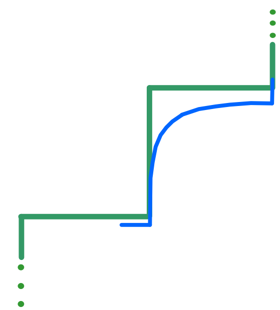
DAC Performance Issues and Concerns



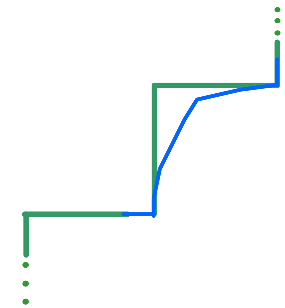
Ideal
(with single LSB steps)



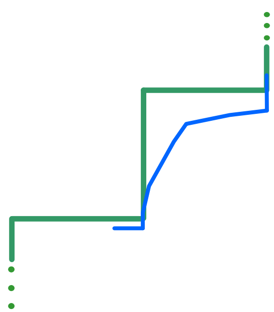
Complete
Linear Settling



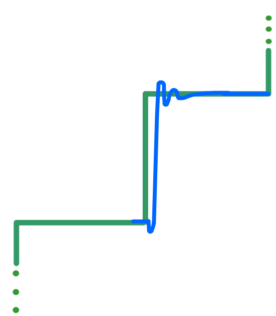
Incomplete
Linear Settling



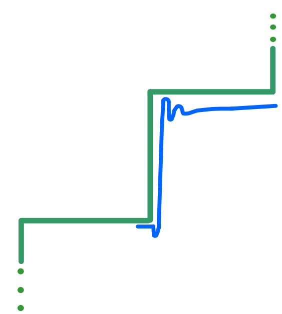
Complete Nonlinear
Settling



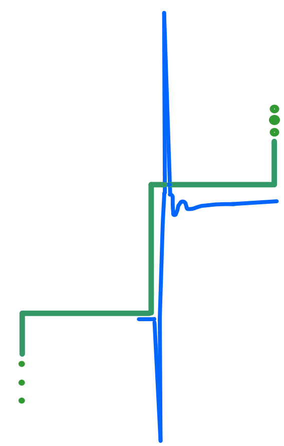
Incomplete
Nonlinear Settling



Complete with glitch

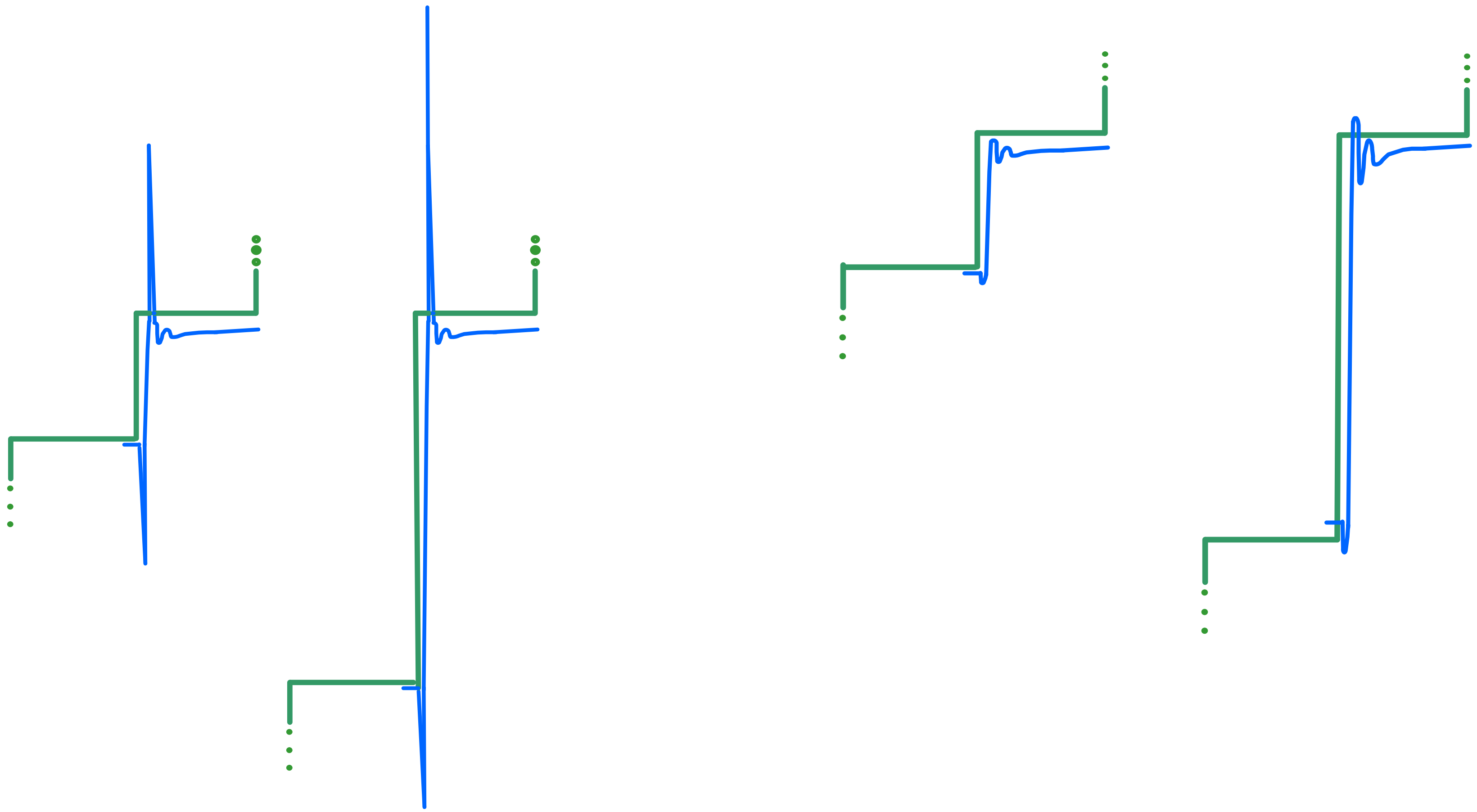


Incomplete with
glitch



Incomplete with big
glitch

DAC Performance Issues and Concerns



Previous code dependent glitches

Previous code dependent settling

Can be strongly dependent on the two code values

Appropriate test bench critical for identifying such issues

DAC Performance Issues and Concerns

Linear settling of DAC outputs do not affect linearity if all have same settling times (for both sampled outputs and overall transient response

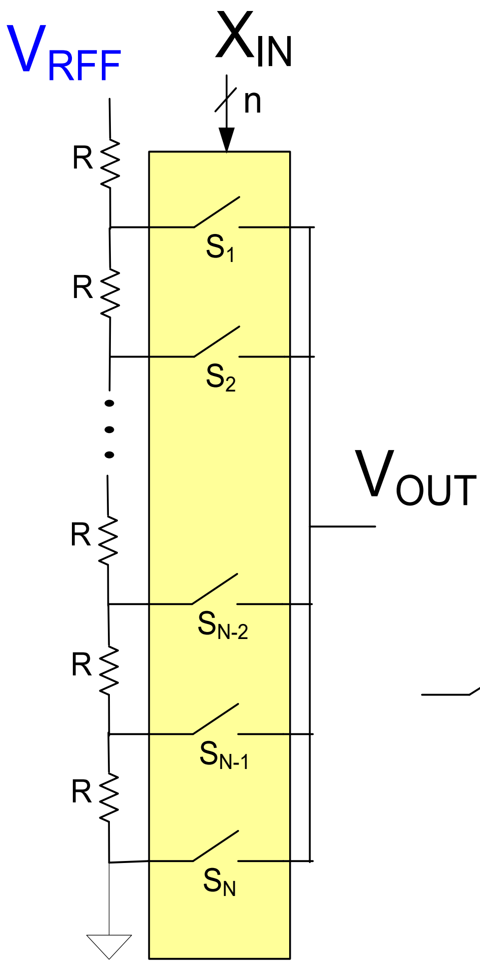
Incomplete nonlinear settling introduces nonlinearities in transient response and usually in settled response

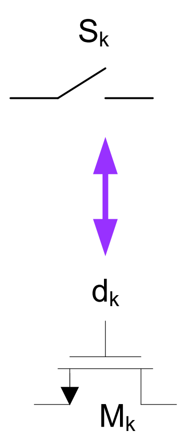
Previous code dependent outputs or settling almost always introduces nonlinearities

Glitches can be many LSB in magnitude and are often previous-code dependent

Glitches in output at transition points do not introduce nonlinearities in settled outputs but may introduce distortion in continuous-time outputs

R-String DAC





Conceptual

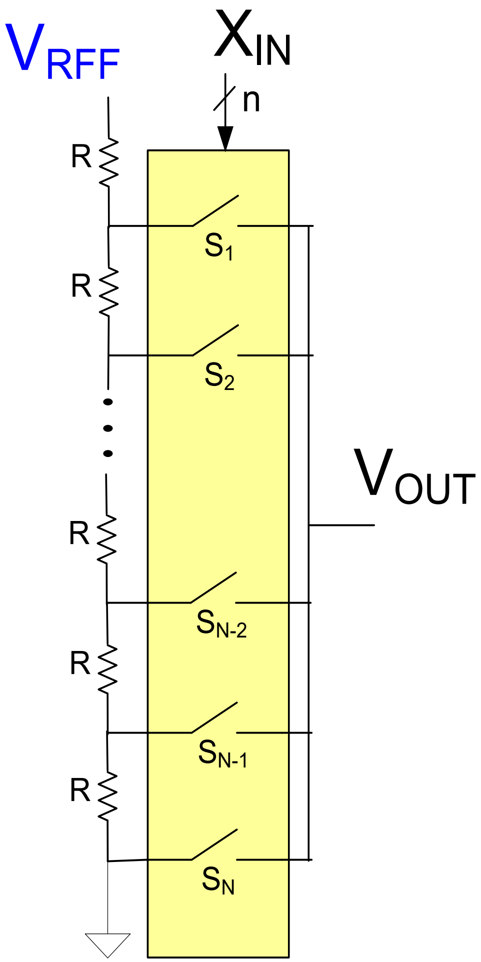
- ❑ Simple structure
- ❑ Inherently monotone
- ❑ Very low DNL
- ❑ Potential for being very fast
- ❑ Low Power Dissipation
- ❑ Widely Used Approach (with appropriate considerations)

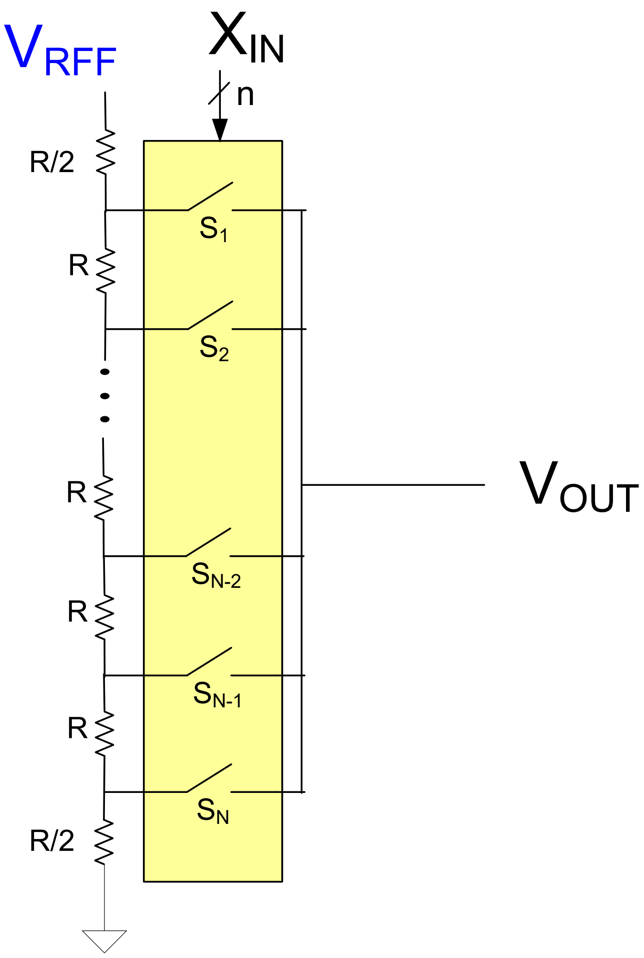
Challenges:

- Managing INL
- Matching (resistors, switches)
- Leakage currents
- Large number of devices for n large (2^n or 2^{n+1} lines)
- Decoder
- Routing thermometer/bubble clocks
- Transients during Boolean transitions
- Glitches
- Switch implementation
- Thevenin impedance facing V_{OUT} highly code dependent

R-String DAC

(minor variant where $V_{OUT}(0,\ldots0) \neq 0$)

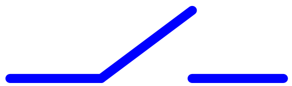




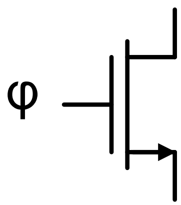
Practical level shift

Switch Implementation

Basic Switch

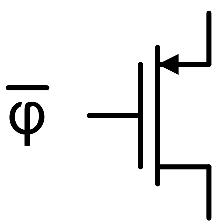


- Large number required for large resolution
- Simple structure often used



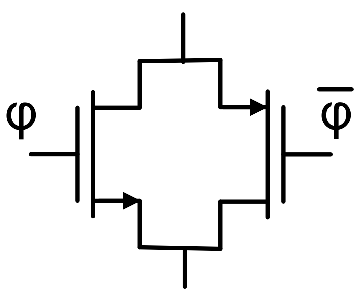
single n-channel device

- Good when switch terminals near gnd
- Will not turn on when terminals near V_{DD}



single p-channel device

- Good when switch terminals near V_{DD}
- Will not turn on when terminals near gnd

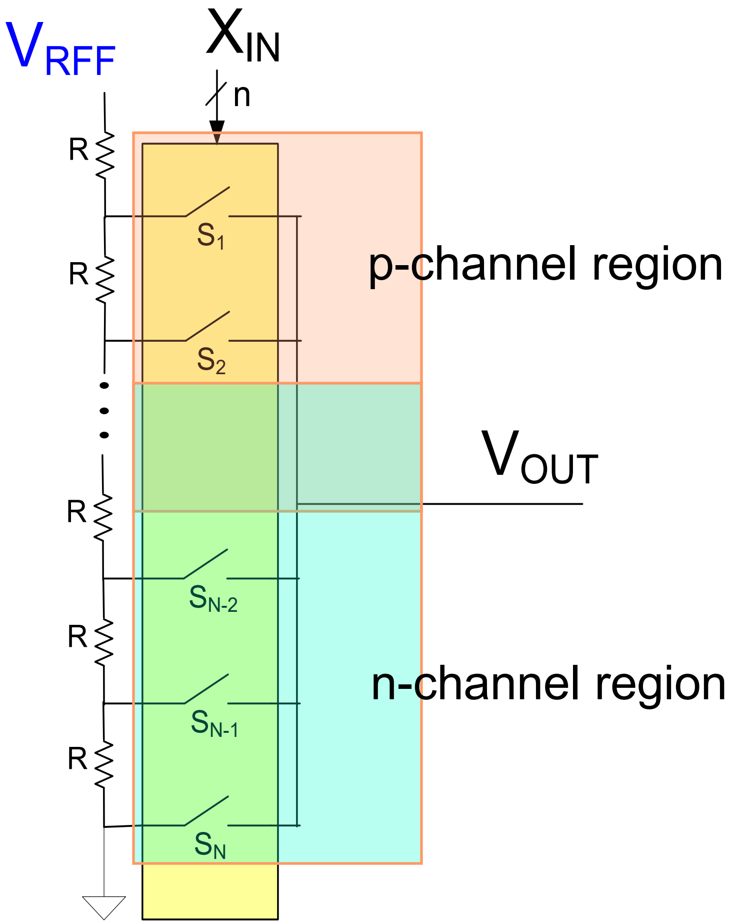


transmission gate switch

- Use devices where cross-over occurs
- Good for both high and low term voltages
- Extra clock signal required
- Try to avoid this complexity

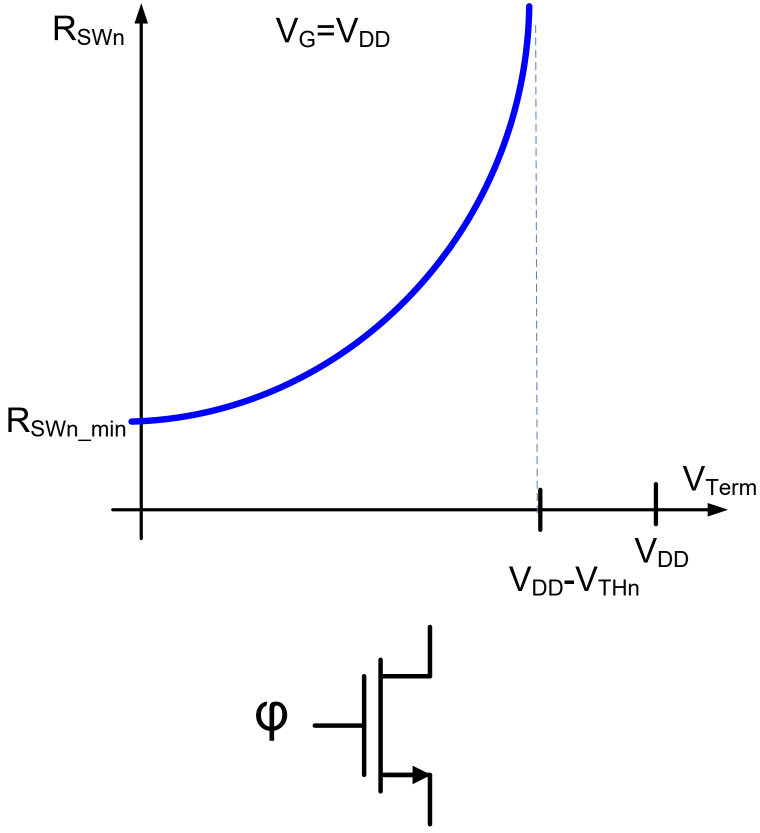
Other switch structures (such as bootstrapped switch) used but not for basic string DACs

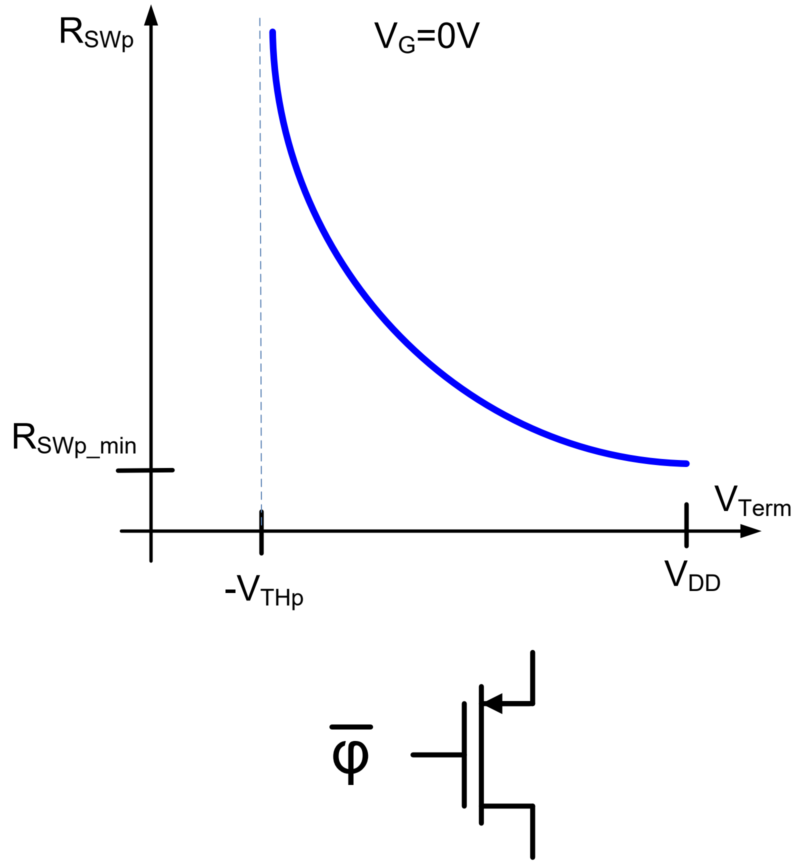
Switch Assignment



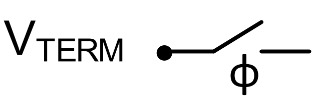
Challenges:

Switch Impedances

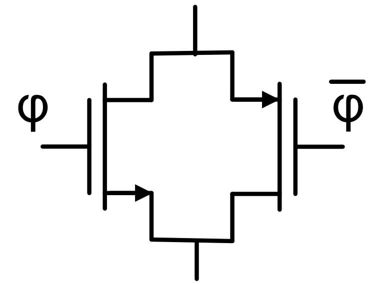


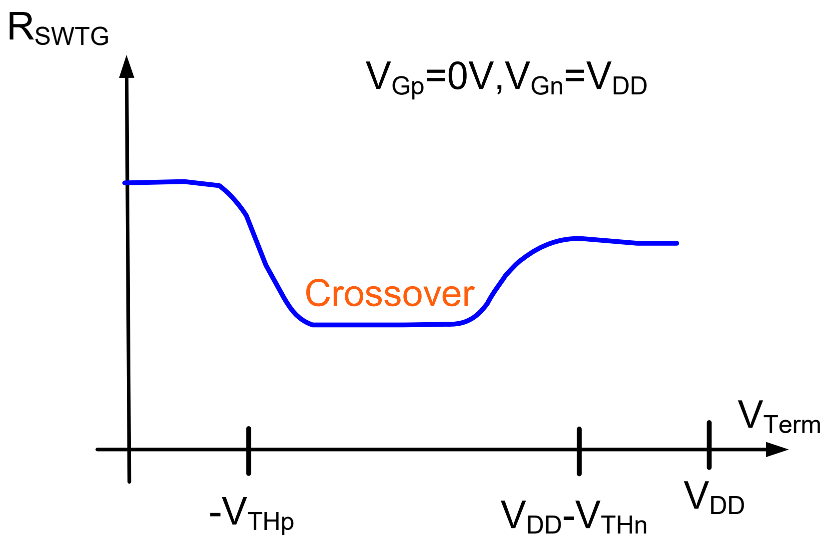


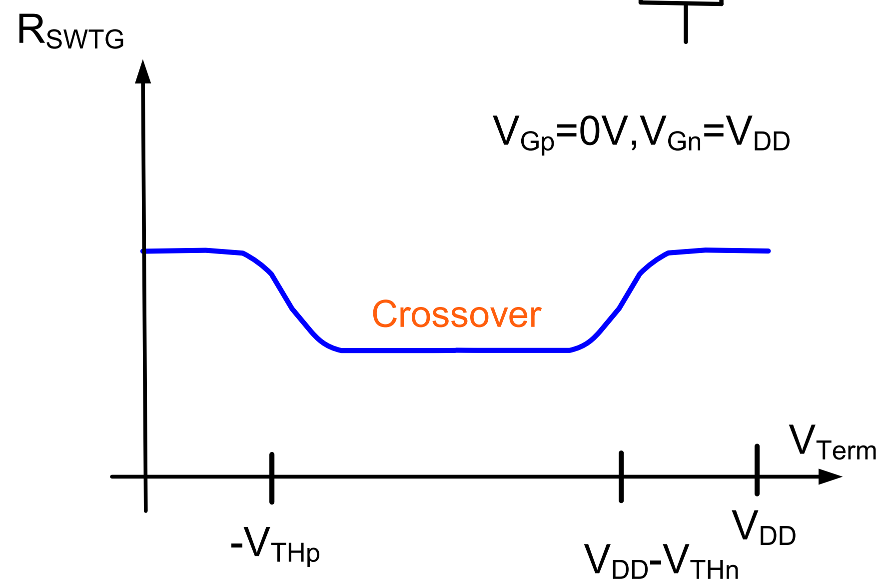
V_{TERM}: Terminal impedance on switch

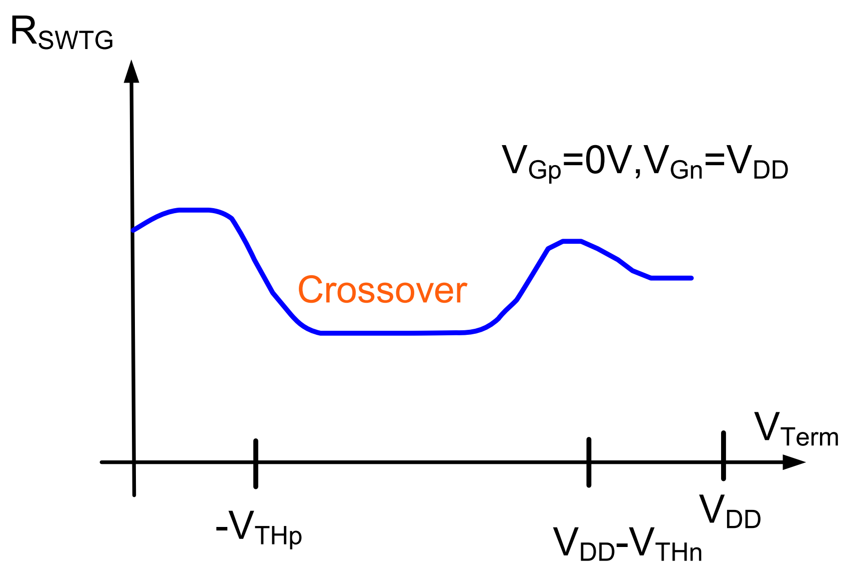


Switch Impedances



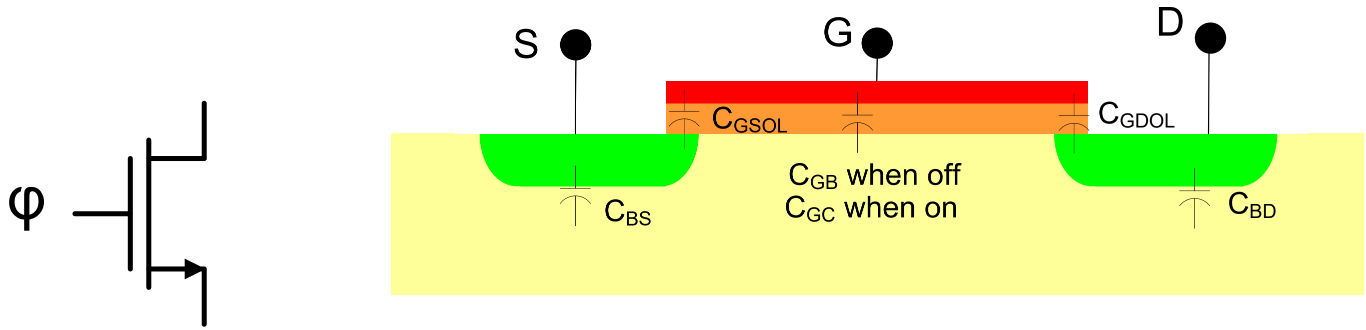


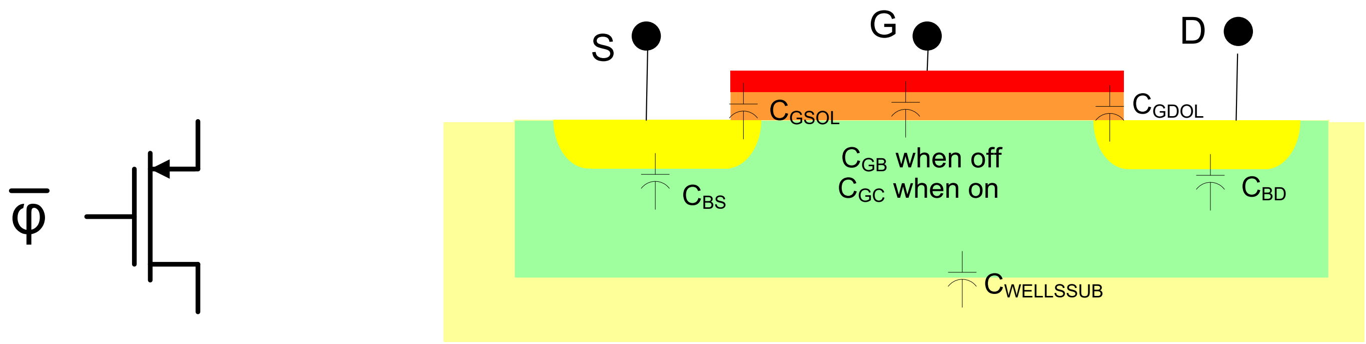




Switch impedance significantly both position and device size dependent

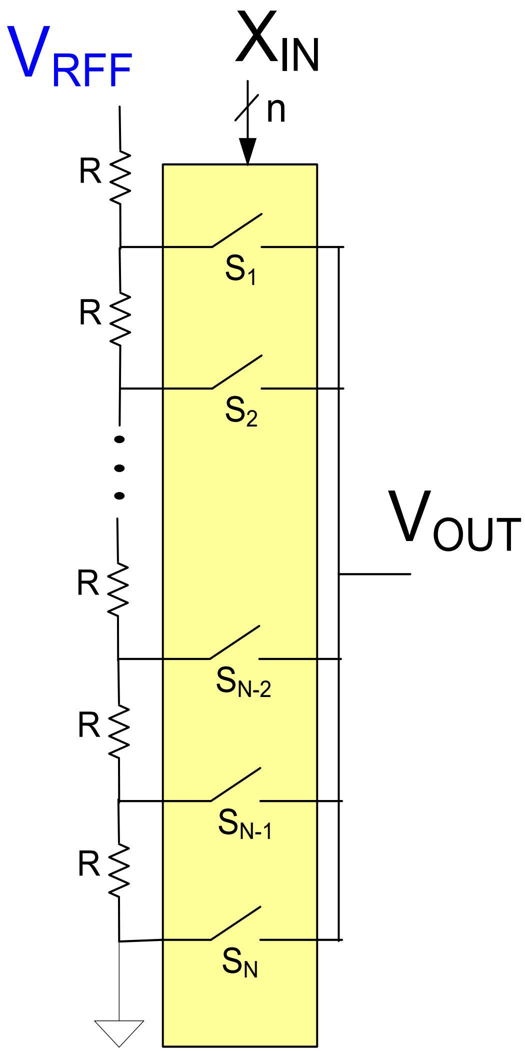
Switch Parasitics





- C_{BD} and C_{BS} can be significant and cause rise-fall times to be position dependent
- C_{GDOL} can cause “kickback” or feed-forward
- C_{GS} can slow turn-on and turn-off time of switch

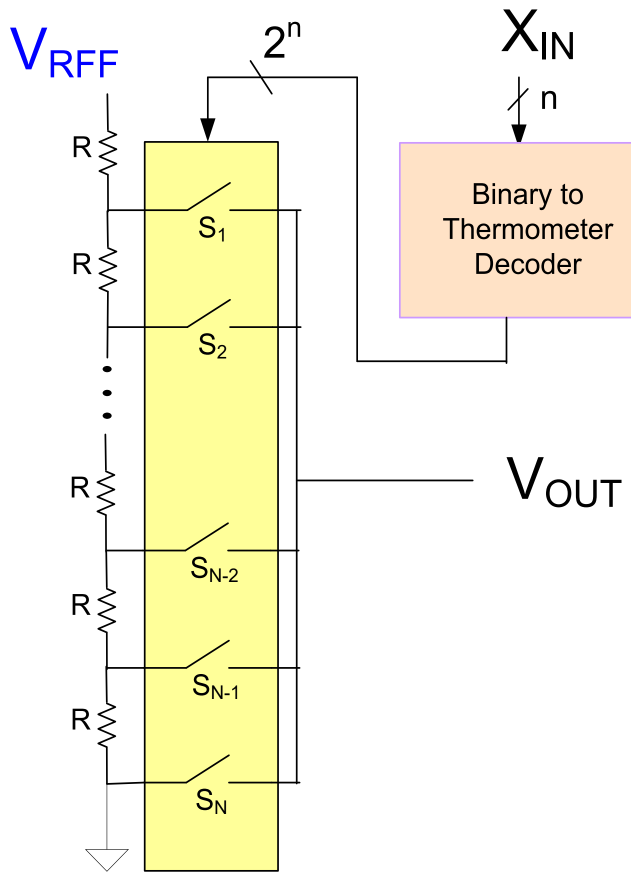
R-String DAC



Additional Challenges:

- Capacitance on V_{OUT} can be large
  - larger for p-channel devices
  - even larger for TG switches
- Switch impedances position dependent
- Kickback from switches to R-string
- Capacitance on each node (though small) of R-string from switch
- Thevenin impedance facing V_{OUT} highly code dependent
- Gradient effects may cause nonlinearities since common-centroid layout may not be practical if n is large

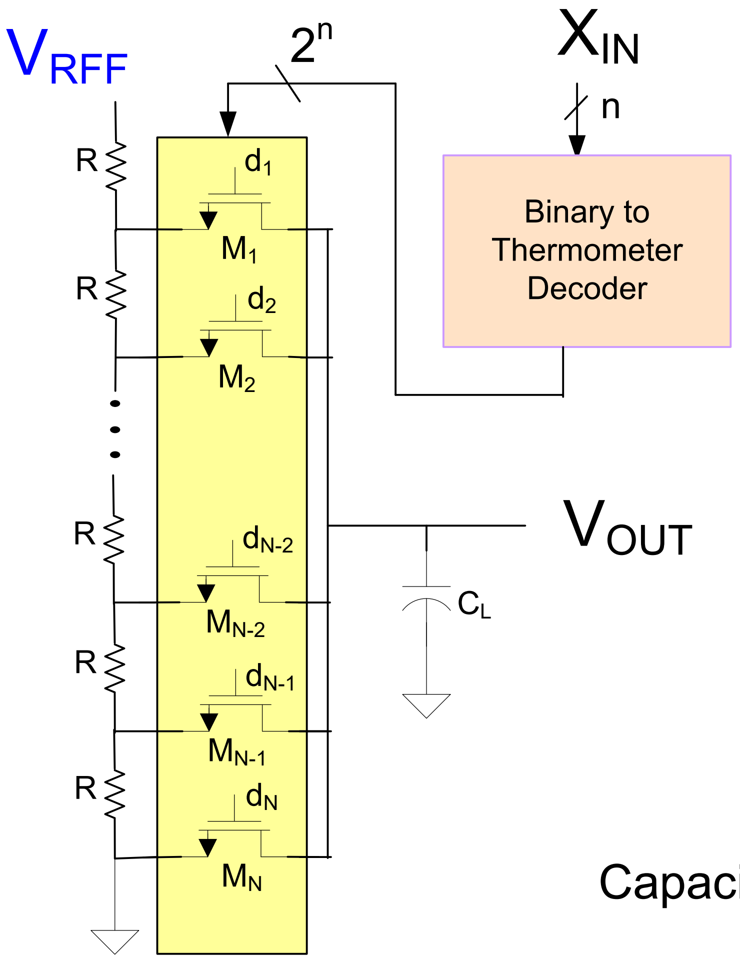
R-String DAC



Additional Challenges

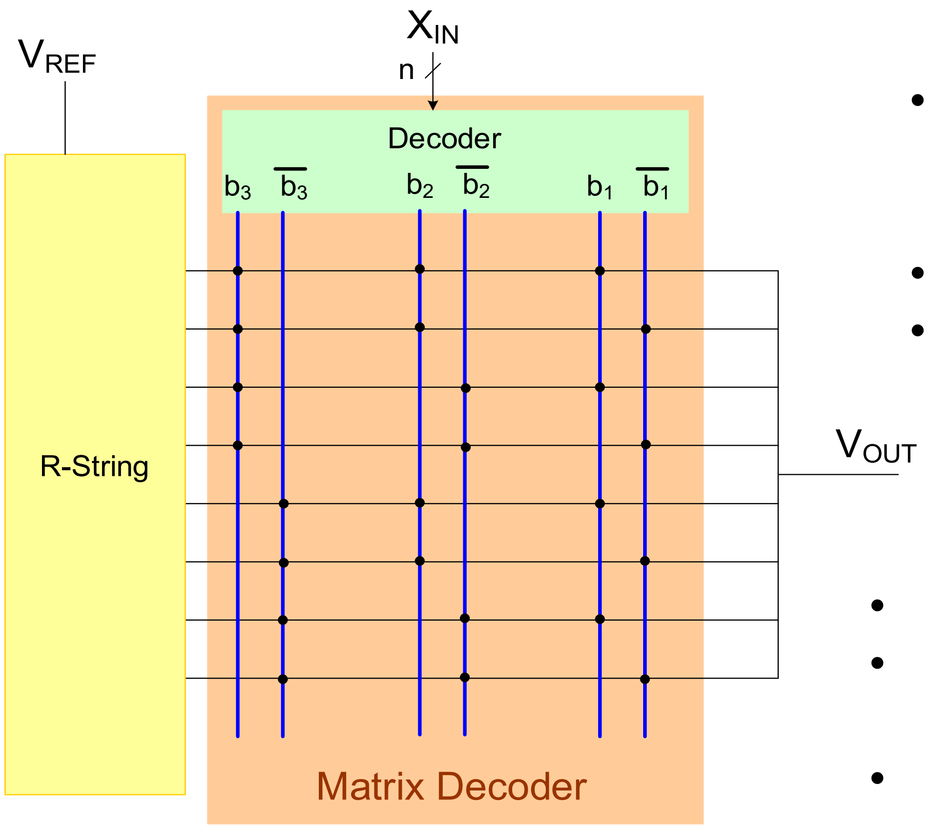
- Delay in Decoder may be significant
- Delay in Decoder may be previous code and current code dependent
- Intermediate undesired Boolean outputs may occur
  - These may cause undesired opening and closing of switches
  - Could momentarily short out taps on R-string
  - Could introduce transients on all nodes of R-string that are code and previous code dependent

R-String DAC



Capacitive loading due to switches

R-String DAC

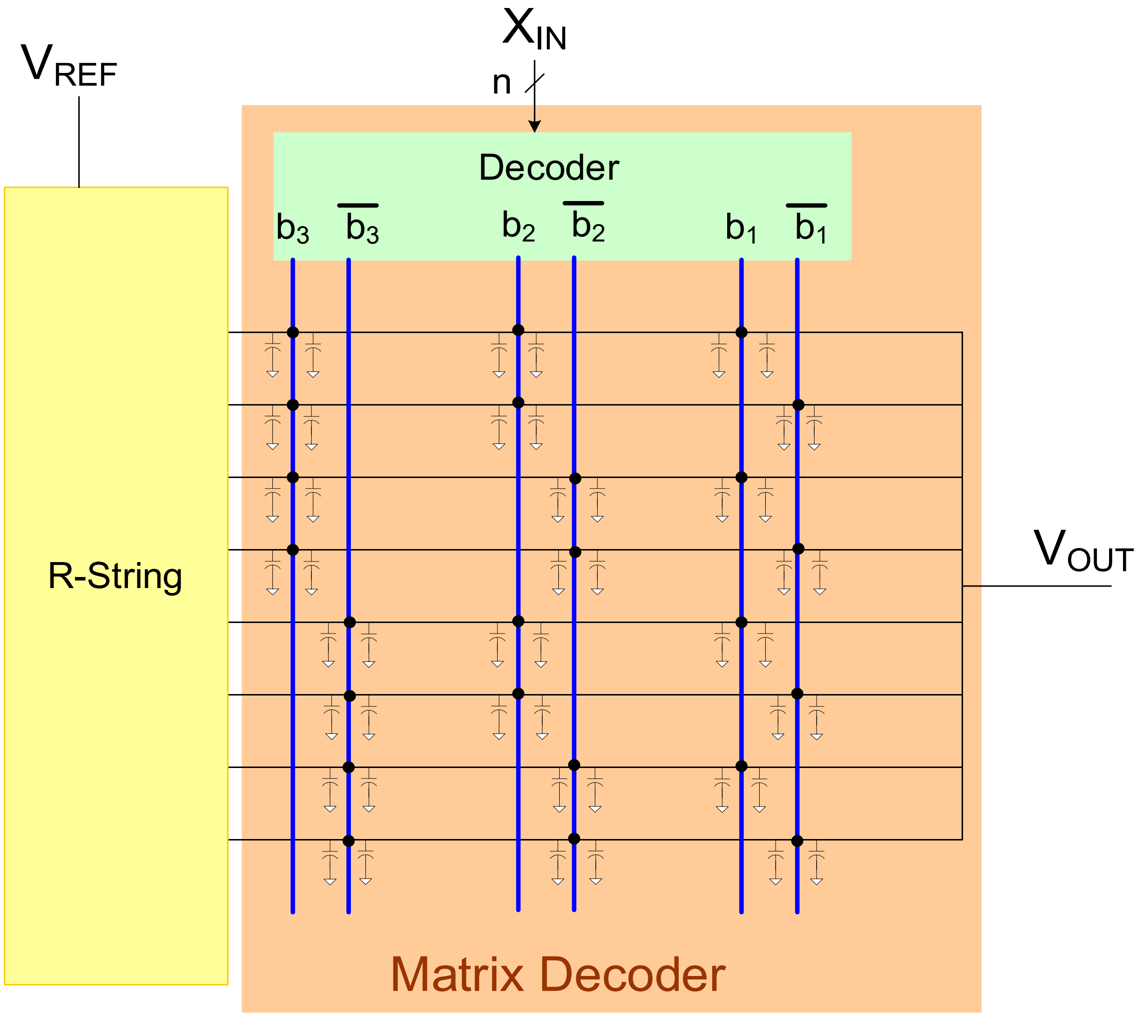


- Uses matrix decoder as analog MUX (don't synthesize decoder)
- Implements binary to decimal conversion with pass transistor analog logic
- Very structured layout
- Interconnection points are switches (combination of n-channel and p-channel)

Challenges

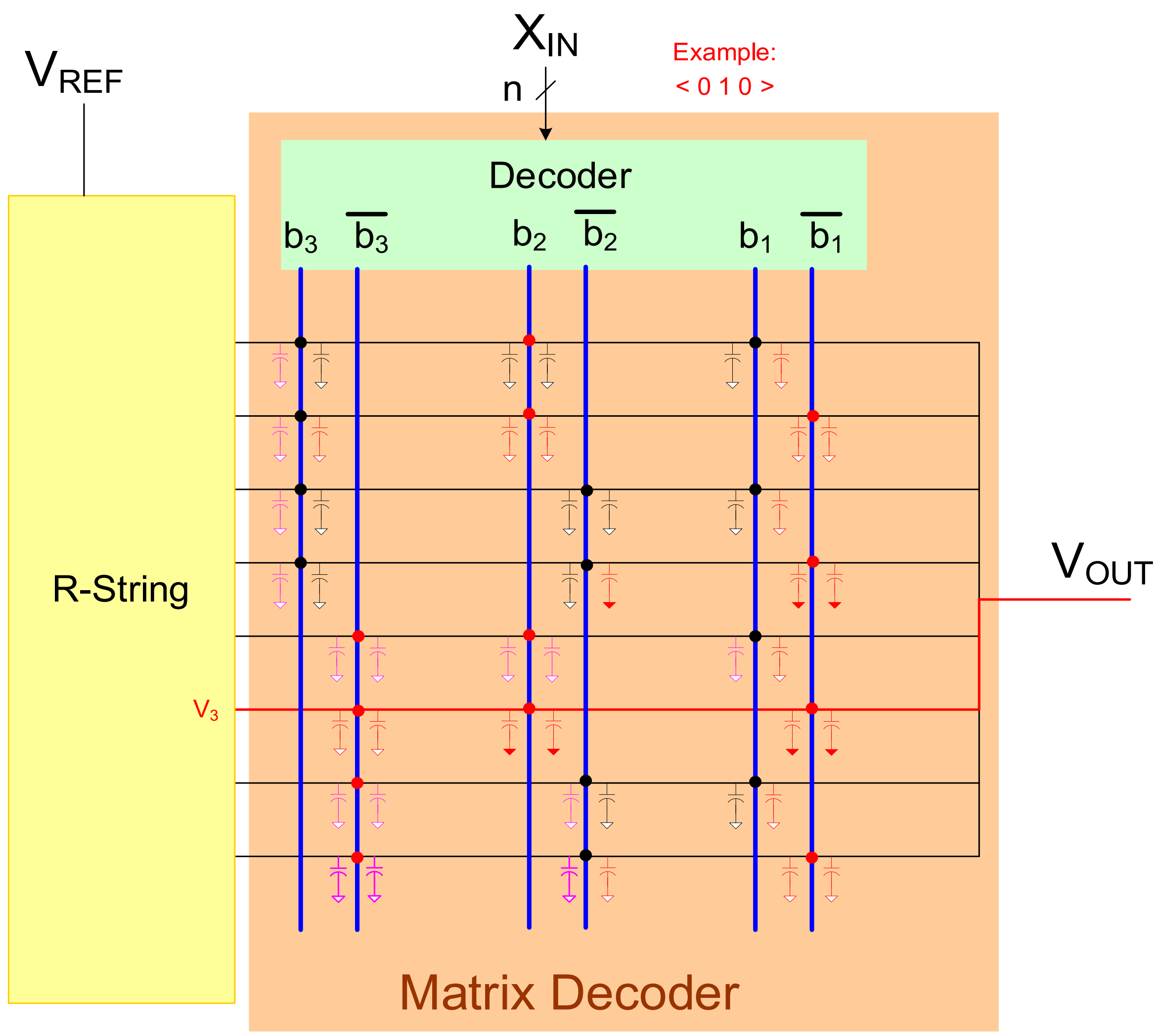
- Still many signals to route
- Large capacitance on V_{OUT} (over 2^{n+1} diff caps)
- Multiple previous code dependencies cause output transition time to be quite unpredictable
- Considerable transients introduced on R-string

R-String DAC



Parasitic Capacitances in Tree Decoder

R-String DAC



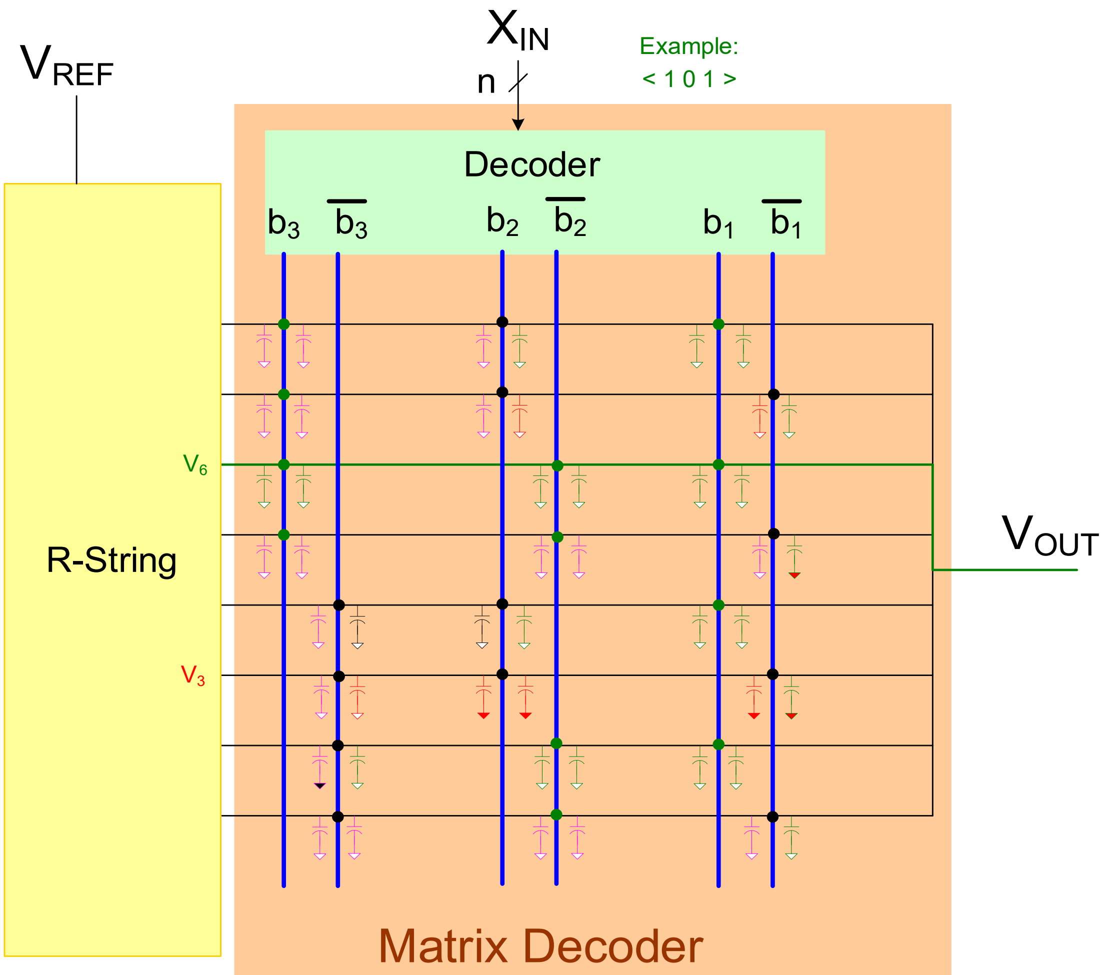
Previous-Code Dependent Settling

Assume all C's (except those on the R-string) initially with 0V

Red denotes V_3, black denotes 0V, Purple some other voltage

R-String DAC

Transition from <010> to <101>



Previous-Code Dependent Settling

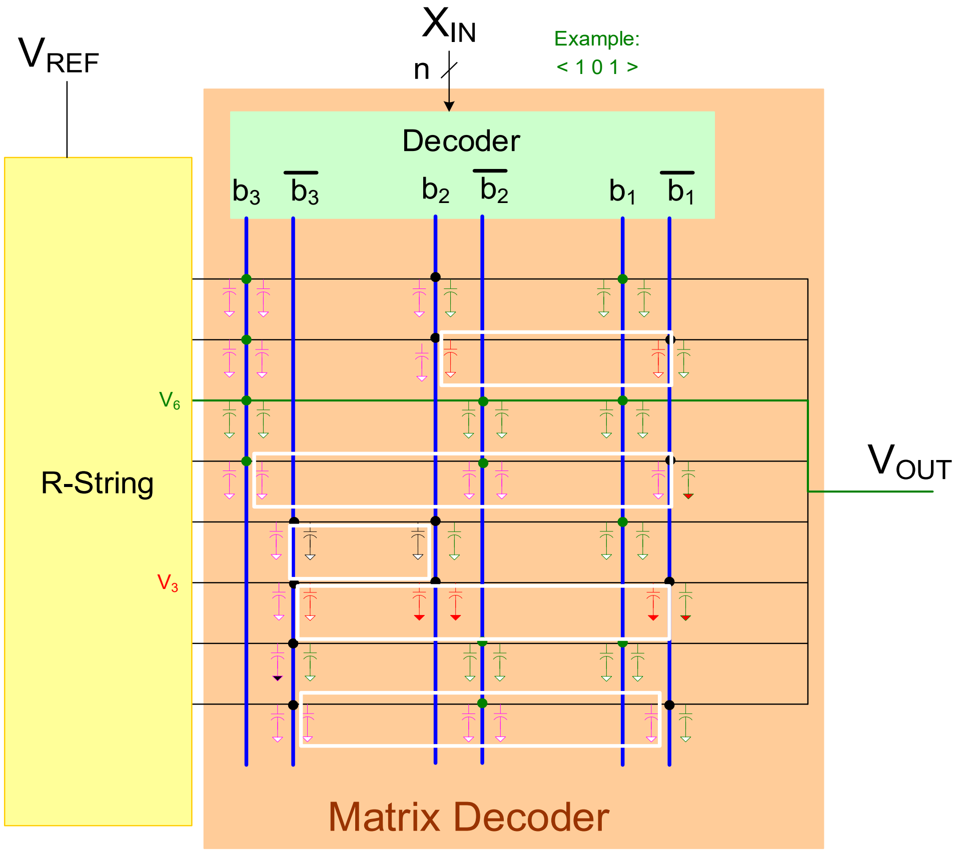
Assume all C's (except those on the R-string) were initially at 0V

Red denotes V_3, green denotes V_6, black denotes 0V, Purple some other voltage

R-String DAC

Transition from <010> to <101>

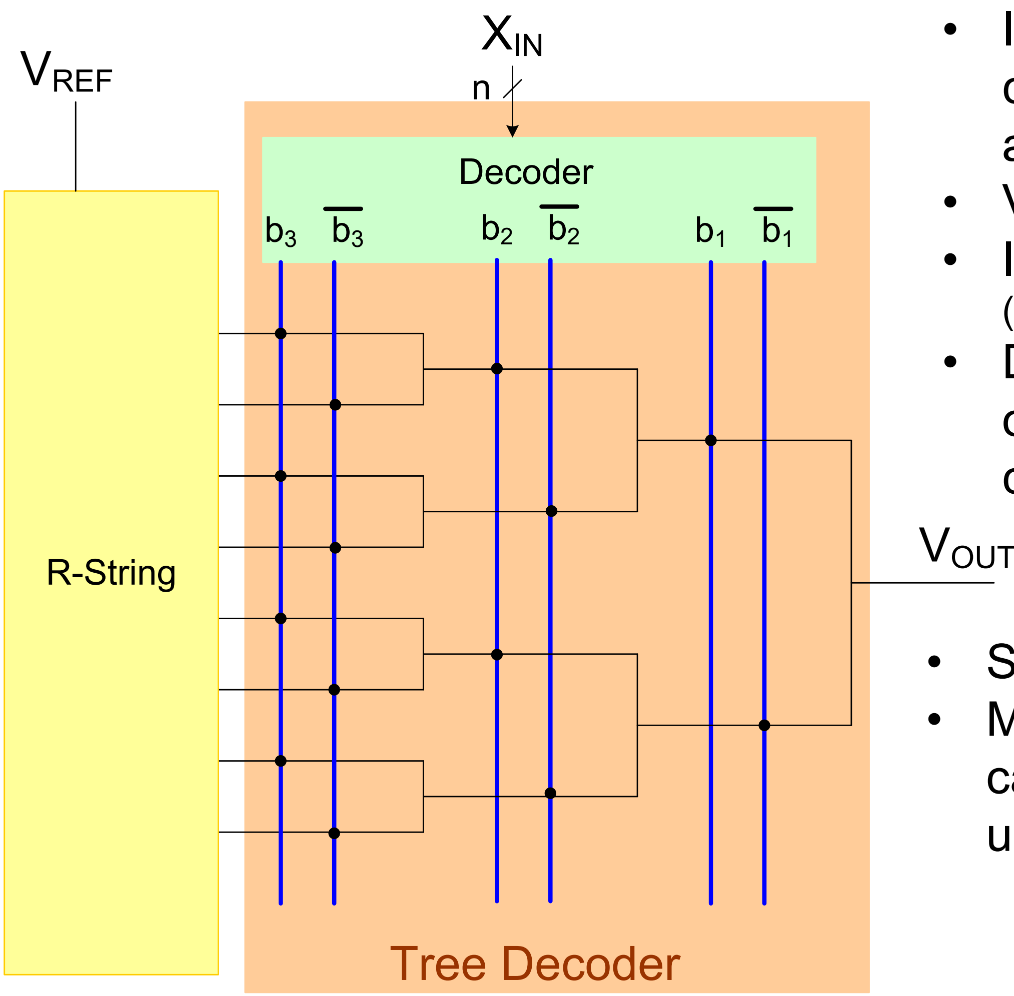
White boxes show capacitors dependent upon previous code <010>



Previous-Code Dependent Settling

- Assume all C's (except those on the R-string) were initially at 0V
- Red denotes V_3, green denotes V_6, black denotes 0V, Purple some other voltage
- Some capacitors may retain values from a previous input for many clock cycles for some inputs resulting I previous-previous dependence of even longer

R-String DAC

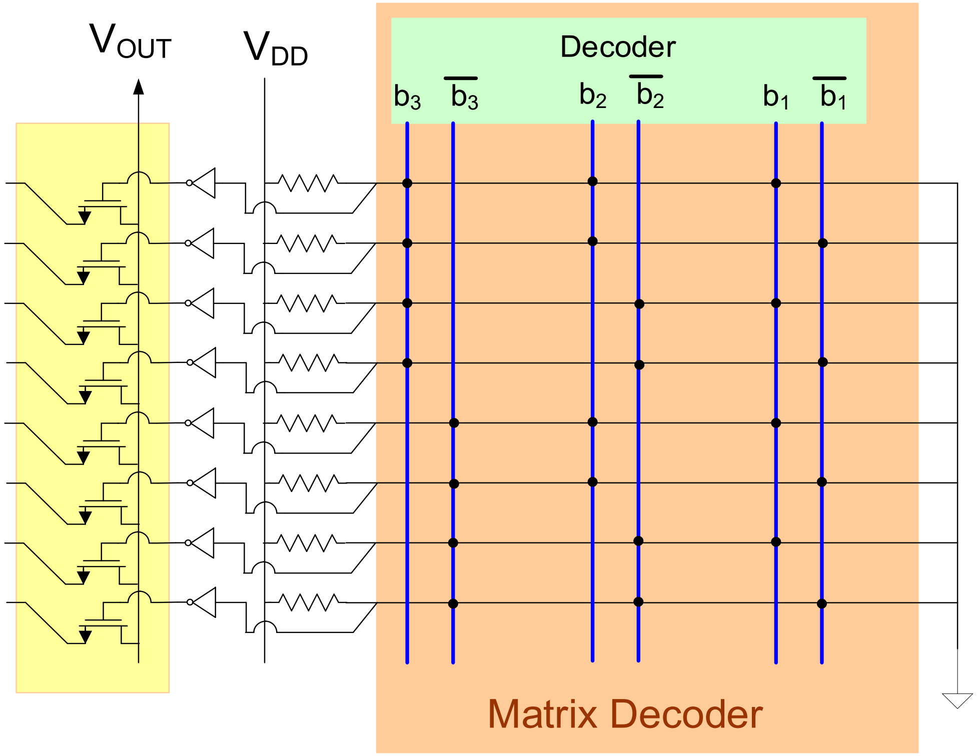


- Uses tree decoder as analog MUX
- Implements binary to decimal conversion with pass transistor analog logic
- Very structured layout
- Interconnection points are switches (combination of n-channel and p-channel)
- Dramatically reduces capacitance on output and switching capacitances

Challenges

- Still many signals to route
- Multiple previous code dependencies cause output transition time to be quite unpredictable

R-String DAC



Tree-Decoder in Digital Domain

Single transistor used at each marked intersection for PTL AND gates

Dramatic reduction in capacitive loading at output

Do the resistors that form part of PTL dissipate any substantial power?

No because only one will be conducting for any DAC output

Will become more complicated if both p-channel and n-channel switches needed

Stay Safe and Stay Healthy !

End of Lecture 12